

DYNAMIC ENGINEERING

150 DuBois St. Suite C, Santa Cruz, CA 95060
831-457-8891 Fax 831-457-4793
sales@dyneng.com www.dyneng.com
Est. 1988

Statement of Volatility for the PCIeBMCX1 and PCIeBPMC

Both designs have similar features – the difference being the number of PCIe lanes and number of LED's.

Devices with memory on the carrier card. This statement does not cover any user installed hardware.

Bridge : Tundra [IDT] Tsi384 Internal registers for configuration, FIFO memory to support link traffic. FIFO memory is continuously rewritten during operation and effectively cleared by this process. FIFO on PCIe lanes includes Four, 128-byte read completion buffers. FIFO on PCI(x) bus is a 4K byte read completion buffer.

Optional EEPROM: normally **not installed**. Memory to provide additional default settings for the bridge device. Programmed via configuration space on host side, not directly user configurable.

No other memory capable devices.

Power cycle or system reset will return to the default settings within the bridge and clear the FIFO. Power cycle will actually clear the FIFO. Reset will return the pointers to the empty position but the data would still be present, just not reachable by design.

To clear the EEPROM a standard 3 pass write cycle would be required. In most cases this device is not installed and therefore not an issue.

