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IpParIo

Driver Package for IP-Parallel-IO Series

Windows 10 WDF Driver Documentation

Developed with Windows Driver Foundation Ver1.19

Revision 1.2
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IpParIo
WDF Device Driver for
IP-Parallel-IO IP Modules

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Introduction

Note: In this document IpPar?? and IP- Parallel-?? refer to one of seven versions of the IP-Parallel-IO hardware. With this release of the unified driver one driver and UserAp reference package support all standard models of IP-Parallel-IO. Two date the TTL and 485 models are covered with the unified driver. The remaining versions use the separated drivers. The Windows support package is updated with each update to remove the old version replacing with the updated unified version. The versions and the I/O distributions are as follows:

Board Type	Driver Name	IO configuration
IP-Parallel-TTL	IpParIo	48 TTL / 0 RS485
IP-Parallel-1	IpPar_1	40 TTL / 4 RS485
IP-Parallel-2	IpPar_2	32 TTL / 8 RS485
IP-Parallel-3	IpPar_3	24 TTL / 12 RS485
IP-Parallel-4	IpPar_4	16 TTL / 16 RS485
IP-Parallel-5	IpPar_5	8 TTL / 20 RS485
IP-Parallel-485	IpParIo	0 TTL / 24 RS485

The IP-PARALLEL-?? driver is a Windows device driver for the IP-Parallel-IO Industry-pack (IP) module from Dynamic Engineering. This driver was developed with the Windows Driver Foundation version 1.19 (WDF) from Microsoft, specifically the Kernel-Mode Driver Framework (KMDF).

The driver is delivered as installed or executable items to be used directly or indirectly by the user. The UserAp code is delivered in source form [C] and is for the purpose of providing a reference to using the driver.

UserAp is a stand-alone code set with a simple, and powerful menu plus a series of “tests” that can be run on the installed hardware. Each of the tests execute calls to the driver, pass parameters and structures, and get results back. With the sequence of calls demonstrated, the functions of the hardware are utilized for loop-back testing. The software is used for manufacturing test at Dynamic Engineering.

The test software can be ported to your application to provide a running start. It is recommended to port the Register Test to your application to get started. The test is simple and will quickly demonstrate the end-to-end operation of your application making calls to the driver and interacting with the hardware.

The menu allows the user to add tests, to run sequences of tests, to run until a failure occurs and stop or to continue, to program a set number of loops to execute and more. The user can add tests to the provided test suite to try out application ideas before committing to your system configuration. In many cases the test configuration will allow faster debugging in a more controlled environment before integrating with the rest of the

system. The test suite is designed to accommodate up to 5 boards. The number of boards can be expanded. See Main.c to increase the number of handles.

The hardware manual defines the pinout, the bitmaps and detailed configurations for each feature of the design. The driver handles all aspects of interacting with the hardware. For added explanations about what some of the driver functions do, please refer to the hardware manual.

We strive to make a useable product, and while we can guarantee operation, we can't foresee all concepts for client implementation. If you have suggestions for extended features, special calls for particular set-ups or whatever please share them with us, [engineering@dyneng.com] and we will consider, and in many cases add them.

When the IP-PARALLEL-?? board is recognized by the IP Carrier Driver, the carrier driver will start the IP- PARALLEL-?? driver which will create a device object for the board. If more than one is found additional copies of the driver are loaded. The carrier driver will load the info storage register on the IP- PARALLEL-?? with the carrier switch setting and the slot number of the IP- PARALLEL-?? device. From within the IP-PARALLEL-?? driver the user can access the switch and slot information to determine the specific device being accessed when more than one is installed.

The integrated version of the UserAp uses the type field within the IDPROM for the installed HW to determine which type is being accessed. The driver displays the correct type in Device Manager. The menu associated with UserAp prints the type at the top of the menu and shows which type of board is tested if the ATP selection is made. Note: some tests require the loop-back to be in place. IP-Debug-IO is used. See the HW manual for details.

The reference software application has a loop to check for devices. The number of devices found, the locations, and device count are printed out at the top of the menu.

IO Control calls (IOCTLs) are used to configure the board and read status. Read and Write calls are used to move data in and out of the device.

Note

This documentation will provide information about all calls made to the driver, and how the driver interacts with the hardware for each of these calls. For more detailed information on the hardware implementation, refer to the IP-Parallel-IO device user manual (also referred to as the hardware manual).

Driver Installation

There are several files provided in each driver package. These files include IpParIo.sys, IpParIo.cat, IpParIo.inf. IpParIoPublic.h is included with UserAp.

IpParIoPublic.h and IpPublic.h are C header files that define the Application Program Interface (API) to the driver. These files are required at compile time by any application that wishes to interface with the driver, but are not needed for driver installation. *Your location will likely be different requiring the link inside the UserAp package to be updated.*

Warning: The appropriate IP carrier driver must be installed before any IP modules can be detected by the system.

Windows 10 Installation

Copy IpPar??.inf, IpPar??.cat, IpPar??.sys and the other IP module drivers to a removable memory device or other accessible location as preferred.

With the IP hardware installed, power-on the host computer.

- Open the ***Device Manager*** from the control panel.
- Under ***Other devices*** there should be an item for each IP module installed on the IP carrier. The label for a module installed in the first slot of the first PCIe3IP carrier would read ***PcieCar0 IP Slot A****.
- Right-click on the first device and select ***Update Driver Software***.
- Insert the removable memory device prepared above if necessary.
- Select ***Browse my computer for driver software***.
- Select ***Browse*** and navigate to the memory device or other location prepared above.
- Select ***Next***. The IpPar?? device driver should now be installed.
- Select ***Close*** to close the update window.
- Right-click on the remaining IP slot icons and repeat the above procedure as necessary.

** If the [Carrier] IP Slot [x] devices are not displayed, click on the Scan for hardware changes icon on the Device Manager tool-bar.*

Driver Startup

Once the driver has been installed it will start automatically when the system recognizes the hardware.

A handle can be opened to a specific board by using the CreateFile() function call and passing in the device name obtained from the system.

The interface to the device is identified using a globally unique identifier (GUID), which is defined in IpPar??Public.h.

The *main.c* file provided with the user test software can be used as an example to show how to obtain a handle to an IpPar?? device.

IO Controls

IOCTL names are of the form IOCTL_IP_PAR_IO_... for “calls” that are common across all versions of the IP-Parallel-IO family. The names are made specific when applied to one version in particular. IOCTL_IP_PAR_485_... for example. For convenience, the IOCTLs are grouped by board type in the Public file as well as the Userap [IOCTL.c and IOCTL.h].

The driver uses IO Control calls (IOCTLs) to configure the device. IOCTLs refer to a single Device Object, which controls a single module. IOCTLs are called using the Win32 function DeviceIoControl() (see below), and passing in the handle to the device opened with CreateFile() (see above). IOCTLs generally have input parameters, output parameters, or both. Often a custom structure is used.

```
BOOL DeviceIoControl(
  HANDLE        hDevice,          // Handle opened with CreateFile()
  DWORD         dwIoControlCode,  // Control code defined in API header file
  LPVOID        lpInBuffer,       // Pointer to input parameter
  DWORD         nInBufferSize,    // Size of input parameter
  LPVOID        lpOutBuffer,      // Pointer to output parameter
  DWORD         nOutBufferSize,   // Size of output parameter
  LPDWORD       lpBytesReturned,  // Pointer to return length parameter
  LPOVERLAPPED  lpOverlapped,     // Optional pointer to overlapped structure
);                                //   used for asynchronous I/O
```

Common IOCTLs

IOCTL_IP_PAR_IO_GET_INFO

Function: Returns the device instance number, driver version, carrier switch value and carrier slot number.
Input: None
Output: DRIVER_IP_DEVICE_INFO structure
Notes: This call does not access the hardware, only stored driver parameters. NewIpCntl indicates that the module's carrier has expanded slot control capabilities. See the definition of DRIVER_IP_DEVICE_INFO below.

```
 //  Driver version and instance/slot information
typedef struct _DRIVER_IP_DEVICE_INFO {
   UCHAR    DriverRev;         // Driver revision
   UCHAR    FirmwareRev;       // Firmware major revision
   UCHAR    FirmwareRevMin;    // Firmware minor revision
   UCHAR    InstanceNum;       // Zero-based device number
   UCHAR    CarrierSwitch;     // 0..0xFF
   UCHAR    CarrierSlotNum;    // 0..7 -> IP slots A, B, C, D, E, F, G or H
   UCHAR    CarDriverRev;      // Carrier driver revision
   UCHAR    CarFirmwareRev;    // Carrier firmware major revision
   UCHAR    CarFirmwareRevMin;// Carrier firmware minor revision
   UCHAR    CarCPLDRev;        //**Used for PCIe carriers only**0xFF for
others
   UCHAR    CarCPLDRevMin;     //**Used for PCIe carriers only**0xFF for
others
   BOOLEAN  Ip32MCapable;      // IP capable of both 8MHz and 32MHz operation
   BOOLEAN  NewIpCntl;         // New IP slot control interface
   WCHAR    LocationString[IP_LOC_STRING_SIZE];
} DRIVER_IP_DEVICE_INFO, *PDRIVER_IP_DEVICE_INFO;
```

IOCTL_IP_PAR_IO_SET_IP_CONTROL

Function: Sets various control parameters for the IP slot the module is installed in.
Input: IP_SLOT_CONTROL structure
Output: None
Notes: Controls the IP clock speed, interrupt enables and data manipulation options for the IP slot that the board occupies. See the definition of IP_SLOT_CONTROL below. For more information refer to the IP carrier hardware manual.

```
typedef struct _IP_SLOT_CONTROL {
   BOOLEAN  Clock32Sel;
   BOOLEAN  ClockDis;
   BOOLEAN  ByteSwap;
   BOOLEAN  WordSwap;
   BOOLEAN  WrIncDis;
   BOOLEAN  RdIncDis;
   UCHAR    WrWordSel;
   UCHAR    RdWordSel;
   BOOLEAN  BsErrTmOutSel;
   BOOLEAN  ActCountEn;
} IP_SLOT_CONTROL, *PIP_SLOT_CONTROL;
```

IOCTL_IP_PAR_IO_GET_IP_STATE

Function: Returns control/status information for the IP slot the module is installed in.
Input: None
Output: IP_SLOT_STATE structure
Notes: Returns the slot control parameters set in the previous call as well as status information for the IP slot that the board occupies. See the definition of IP_SLOT_STATE below.

```
typedef struct _IP_SLOT_STATE {
   BOOLEAN  Clock32Sel;
   BOOLEAN  ClockDis;
   BOOLEAN  ByteSwap;
   BOOLEAN  WordSwap;
   BOOLEAN  WrIncDis;
   BOOLEAN  RdIncDis;
   UCHAR    WrWordSel;
   UCHAR    RdWordSel;
   BOOLEAN  BsErrTmOutSel;
   BOOLEAN  ActCountEn;
 // Slot Status
   BOOLEAN  IpInt0En;
   BOOLEAN  IpInt1En;
   BOOLEAN  IpBusErrIntEn;
   BOOLEAN  IpInt0Actv;
   BOOLEAN  IpInt1Actv;
   BOOLEAN  IpBusError;
   BOOLEAN  IpForceInt;
   BOOLEAN  WrBusError;
   BOOLEAN  RdBusError;
} IP_SLOT_STATE, *PIP_SLOT_STATE;
```

IOCTL_IP_PAR_IO_SET_BASE_CONFIG

Function: Sets configuration parameters in the base control register.
Input: IP_PAR_IO_BASE_CONFIG structure
Output: None
Notes: Controls the output data latch behavior, the timer/counter A and B interrupt enables and enables the square wave output on the upper data bit. The output data latch can be set to enable, disable or auto. When in auto the outputs from all data registers are enabled onto the output bus simultaneously after each data update call. See the definition of IP_PAR_IO_BASE_CONFIG below. Bit definitions can be found under the 'BASE_CNTL' section under Register Definitions in the Hardware manual.

```
typedef struct _IP_PAR_IO_BASE_CONFIG {
   OUT_SEL  Outen;
   BOOLEAN  CntTmrAIntEn;
   BOOLEAN  CntTmrAWaveEn;
   BOOLEAN  CntTmrBIntEn;
} IP_PAR_IO_BASE_CONFIG, *PIP_PAR_IO_BASE_CONFIG;
```

IOCTL_IP_PAR_IO_GET_BASE_CONFIG

Function: Returns the configuration of the base control register.
Input: None
Output: IP_PAR_IO_BASE_CONFIG structure
Notes: Returns the values set in the previous call.

IOCTL_IP_PAR_IO_REGISTER_EVENT

Function: Registers an event to be signaled when an interrupt occurs.
Input: Handle to Event object
Output: None
Notes: The caller creates an event with CreateEvent() and supplies the handle returned from that call as the input to this IOCTL. The driver then obtains a system pointer to the event and signals the event when an interrupt is serviced. The user interrupt service routine waits on this event, allowing it to respond to the interrupt. In order to un-register the event, set the event handle to NULL while making this call.

IOCTL_IP_PAR_IO_ENABLE_INTERRUPT

Function: Enables the master interrupt.
Input: None
Output: None
Notes: Sets the master interrupt enable, leaving all other bit values in the IPPAR??_BASE register unchanged. This IOCTL is used in the user interrupt processing function to re-enable the interrupts after they were disabled in the driver interrupt service routine. This allows that function to enable the interrupts without knowing the particulars of the other configuration bits.

IOCTL_IP_PAR_IO_DISABLE_INTERRUPT

Function: Disables the master interrupt.
Input: None
Output: None
Notes: Clears the master interrupt enable, leaving all other bit values in the IPPAR??_BASE register unchanged. This IOCTL is used when interrupt processing is no longer desired. Usually not needed as it is cleared in the DPC/ISR.

IOCTL_IP_PAR_IO_ENABLE_CARRIER_INTERRUPT

Function: Enables the IP Slot Interrupt to pass through the carrier to the system
Input: None
Output: None
Notes: Sets the carrier slot interrupt enable, leaving all other bit values unchanged. This IOCTL is used in the user interrupt processing function to re-enable the interrupts after they were disabled in the driver interrupt service routine. This allows that function to enable the interrupts without knowing the particulars of the other configuration bits.

IOCTL_IP_PAR_IO_DISABLE_CARRIER_INTERRUPT

Function: Disables the master interrupt.
Input: None
Output: None
Notes: Clears the master interrupt enable, leaving all other bit values in the control register on the carrier unchanged. This IOCTL is used when interrupt processing is no longer desired. Usually not needed as it is cleared in the DPC/ISR.

IOCTL_IP_PAR_IO_FORCE_INTERRUPT

Function: Causes a system interrupt to occur.
Input: None
Output: None
Notes: Causes an interrupt to be asserted on the IP bus. This IOCTL is used for development, to test interrupt processing.

IOCTL_IP_PAR_IO_GET_ISR_STATUS

Function: Returns the interrupt status and vector read in the last ISR.
Input: None
Output: IPPAR??_INT_STAT structure See IpParIoPublic.h
Notes: The status contains the contents of the INT_STAT register read in the last ISR execution, plus the Filtered data and vector values. If bit 12 is set, it indicates a bus error occurred for this IP slot.

```
typedef struct _IP_PAR_IO_ISR_STAT {
   USHORT   InterruptStatus;
   USHORT   InterruptVector;
   USHORT   FilteredData0;
   USHORT   FilteredData1;
   USHORT   FilteredData2;
} IP_PAR_IO_ISR_STAT, *PIP_PAR_IO_ISR_STAT;
```

IOCTL_IP_PAR_IO_GET_STATUS

Function: Returns the status bits in the INT_STAT register.
Input: None
Output: unsigned short int

IOCTL_IP_PAR_IO_GET_PROM

Function: Returns the IDPROM basic information
Input: None
Output: IP_IDENTITY structure. See IpPublic.h

```
typedef struct _IP_IDENTITY {
   UCHAR    IpManuf;
   UCHAR    IpModel;
   UCHAR    IpRevision;
   UCHAR    IpCustomer;
   USHORT   IpVersion;
} IP_IDENTITY, *PIP_IDENTITY;
```

IOCTL_IP_PAR_IO_SET_VECTOR

Function: Sets the value of the interrupt vector.
Input: unsigned character
Output: None
Notes: This value will be driven onto the low byte of the data bus in response to an INT_SEL strobe, which is used in vectored interrupt cycles. This value will be read in the interrupt service routine and stored for future reference.

IOCTL_IP_PAR_IO_GET_VECTOR

Function: Returns the current interrupt vector value.
Input: None
Output: unsigned character
Notes:

IOCTL_IP_PAR_IO_SET_COUNTER_PRELOAD

Function: Stores a value to be loaded into the A-Counter when a new count is loaded.
Input: unsigned long int
Output: None
Notes: The A-Counter counts down from the loaded count value. When it reaches zero, this count is re-loaded and an interrupt will be generated if the Counter A interrupt is enabled.

IOCTL_IP_PAR_IO_GET_COUNTER_PRELOAD

Function: Returns the value stored in the A-Counter preload registers.
Input: None
Output: unsigned long int
Notes: Returns the value written with the previous call.

IOCTL_IP_PAR_IO_SET_TIMER_MASK

Function: Stores a value in the B-Timer mask registers
Input: unsigned long int
Output: None
Notes: The B-Timer counts up from zero. When a counter bit is high that corresponds to a bit that asserted in the mask register an interrupt will be generated if the Timer B interrupt is enabled.

IOCTL_IP_PAR_IO_GET_TIMER_MASK

Function: Returns the value stored in the B-Timer mask registers.
Input: None
Output: unsigned long int
Notes: Returns the value written with the previous call.

IOCTL_IP_PAR_IO_LOAD_COUNTER

Function: Causes the A-Counter to be loaded with the preload value.
Input: None
Output: None
Notes:

IOCTL_IP_PAR_IO_CLEAR_TIMER

Function: Clears the B-Timer count to zero.
Input: None
Output: None
Notes:

IOCTL_IP_PAR_IO_GET_TIMER_COUNT

Function: Reads the current value of the Timer B count.
Input:
Output: unsigned long int
Notes: The hold count bit is automatically set before the count is read and cleared afterward. This guarantees that a consistent count is read since two accesses are required to read all 32 bits.

485 IOCTLs

IOCTL_IP_PAR_485_SET_485_DIR

Function: Sets the directions for the RS485 drivers on the board.
Input: ULONG
Output: None
Notes: There are 24 RS485 transceivers on the -485 version. 23-0 are valid control bits. Driver auto alters the valid field into accesses to the appropriate control registers. A one in a bit position corresponds to setting that driver to be an output, while a zero corresponds to an input. See CNTL0, CNTL1, and CNTL2 for the specific hardware in the hardware manual for more details.

IOCTL_IP_PAR_485_GET_485_DIR

Function: Returns the direction bits for the RS485 drivers on the board.
Input: None
Output: ULONG
Notes: Returns the bits set in the previous call.

IOCTL_IP_PAR_485_SET_485_DATA

Function: Sets the value of the RS485 outputs on the board.
Input: ULONG
Output: None
Notes: 23-0 are valid data bits. Driver auto alters the valid field into accesses to the appropriate control registers. See CNTL0, CNTL1, and CNTL2 for the specific hardware in the hardware manual for more details.

IOCTL_IP_PAR_485_GET_485_DATA

Function: Returns the state of the RS485 bits in the output data register.
Input: None
Output: ULONG
Notes: Returns the data stored in the Data register. Not the external data.

IOCTL_IP_PAR_485_SET_485_INT_EN

Function: Selects which RS485 inputs can cause an interrupt.
Input: ULONG
Output: None
Notes: This call defines the mask of which of the RS485 input lines will be enabled to cause an interrupt when the specified conditions are met (1 = enabled, 0 = disabled). 23-0 are valid. Driver auto alters the valid field into accesses to the appropriate control registers. See Int_en0, Int_en1, and Int_en2 in the hardware manual for more details.

IOCTL_IP_PAR_485_GET_485_INT_EN

Function: Returns the interrupt enable value set in the previous call.
Input: None
Output: unsigned long int
Notes: The number of valid bits varies with the number of RS485 I/O lines. This call is not valid on the IP-Parallel-TTL board as it has no RS485 drivers.

IOCTL_IP_PAR_485_SET_485_EDGE_LEVEL

Function: Selects whether an RS485 input is edge or level sensitive.
Input: ULONG
Output: None
Notes: Determines whether the interrupt for each of the enabled RS485 input lines will respond to a static logic level or a transition between levels (1 = edge, 0 = level). 23-0 are valid. Driver auto alters the valid field into accesses to the appropriate control registers. See Edg_Lvl0, Edg_Lvl1, and Edg_Lvl2 in the hardware manual for more details.

IOCTL_IP_PAR_485_GET_485_EDGE_LEVEL

Function: Returns the interrupt edge/level values set in the previous call.
Input: None
Output: ULONG
Notes: Returns the value stored in the registers.

IOCTL_IP_PAR_485_SET_485_POLARITY

Function: Selects whether an RS485 input is active high or active low.
Input: ULONG
Output: None
Notes: Determines the polarity of the level or edge to which the interrupt for each of the input lines will respond (1 = inverted: active low or falling edge, 0 = non-inverted: active high or rising edge). 23-0 are valid. Driver auto alters the valid field into accesses to the appropriate control registers. See Pol0, Pol1, and Pol2 in the hardware manual for more details.

IOCTL_IP_PAR_485_GET_485_POLARITY

Function: Returns the interrupt polarity values set in the previous call.
Input: None
Output: ULONG
Notes: Returns the value stored in the registers.

IOCTL_IP_PAR_485_READ_DIRECT

Function: Reads the input data bus directly.
Input: None
Output: ULONG
Notes: This call reads the raw real-time input data from the RS485 input lines. 23-0 are valid. Driver auto alters the valid field into accesses to the appropriate control registers. See Datain_dir0, Datain_dir1, and Datain_dir2 in the hardware manual for more details.

IOCTL_IP_PAR_485_READ_FILTERED

Function: Reads the filtered input data.
Input: None
Output: ULONG
Notes: This call reads the contents of the interrupt latches after the enable mask, edge/level, and polarity bits have been applied. A one means that the specified conditions for that bit have been met. The latched bits are automatically cleared when read by this call. 23-0 are valid. Driver auto alters the valid field into accesses to the appropriate control registers. See Datain_fil0, Datain_fil1, and Datain_fil2 in the hardware manual for more details.

TTL IOCTLs

IOCTL_IP_PAR_TTL_SET_TTL_DATA

Function: Sets the value of the TTL outputs on the board.
Input: IP_PAR_BITS structure
Output: None
Notes: 47-0 are valid bit positions. Driver auto arranges to match 16 bit registers. See the definition of IP_PAR_TTL_BITS below. Note that this same structure is used for all IOCTLs that concern TTL data. See CNTL0, CNTL1, and CNTL2 for the specific hardware in the hardware manual for more details.

```
typedef struct _IP_PAR_BITS
{
   ULONG    LoWord;  // 31-0
   ULONG    HiWord;  // x0000 47-32
} IP_PAR_BITS, *PIP_PAR_BITS;
```

IOCTL_IP_PAR_TTL_GET_TTL_DATA

Function: Returns the state of the TTL outputs in the output data register.
Input: None
Output: IP_PAR_BITS structure
Notes: 47-0 are valid. See the definition of IP_PAR_TTL_BITS above.

IOCTL_IP_PAR_TTL_SET_TTL_INT_EN

Function: Selects which TTL inputs can cause an interrupt.
Input: IP_PAR_BITS structure
Output: None
Notes: This call defines the mask of which of the TTL input lines will be enabled to cause an interrupt when the specified conditions are met (1 = enabled, 0 = disabled). 47-0 are valid. Driver auto arranges to match 16 bit registers. See Int_en0, Int_en1, and Int_en2 in the hardware manual for more details.

IOCTL_IP_PAR_TTL_GET_TTL_INT_EN

Function: Returns the interrupt enable values set in the previous call.
Input: None
Output: IP_PAR_BITS structure
Notes: Returns register values. Driver auto arranges to match 16 bit registers. See the definition of IP_PAR_TTL_BITS above.

IOCTL_IP_PAR_TTL_SET_TTL_POLARITY

Function: Selects whether a TTL input is active high or active low.
Input: IP_PAR_BITS structure
Output: None
Notes: Determines the polarity of the level or edge to which the interrupt for each of the input lines will respond (1 = inverted: active low or falling edge, 0 = non-inverted: active high or rising edge). 47-0 are valid. Driver auto arranges to match 16 bit registers. See the definition of IP_PAR_BITS. See Pol0, Pol1, and Pol2 in the hardware manual for more details.

IOCTL_IP_PAR_TTL_GET_TTL_POLARITY

Function: Returns the interrupt polarity values set in the previous call.
Input: None
Output: IP_PAR_BITS structure

IOCTL_IP_PAR_TTL_SET_TTL_EDGE_LEVEL

Function: Selects whether a TTL input is edge-sensitive or level sensitive.
Input: IP_PAR_BITS structure
Output: None
Notes: Determines whether the interrupt for each of the enabled TTL input lines responds to a static logic level or a transition between levels (1 = edge, 0 = level). 47-0 are valid. Driver auto arranges to match 16 bit registers. See the definition of IP_PAR_TTL_BITS above. See Edg_Lvl0, Edg_Lvl1, and Edg_Lvl2 in the hardware manual for more details.

IOCTL_IP_PAR_TTL_GET_TTL_EDGE_LEVEL

Function: Returns the interrupt edge/level values set in the previous call.
Input: None
Output: IP_PAR_BITS structure
Notes: Returns register value. See the definition of IP_PAR_TTL_BITS above.

IOCTL_IP_PAR_TTL_READ_DIRECT

Function: Reads the input data bus directly.
Input: None
Output: IP_PAR_BITS structure
Notes: This call reads the raw real-time input data from the TTL input lines. 47-0 are valid. Driver auto arranges to match 16 bit registers. See Datain_dir0, Datain_dir1, and Datain_dir2 in the hardware manual for more details.

IOCTL_IP_PAR_TTL_READ_FILTERED

Function: Reads the filtered input data.
Input: None
Output: IP_PAR_BITS structure
Notes: This call reads the contents of the interrupt latches after the enable mask, edge/level, and polarity bits have been applied. A one means that the specified conditions for that bit have been met. The latched bits are automatically cleared when read by this call. 47-0 are valid. Driver auto arranges to match 16 bit registers. See Datain_fil0, Datain_fil1, and Datain_fil2 in the hardware manual for more details.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the driver is at fault. The driver has gone through extensive testing, and in most cases it will be “cockpit error” rather than an error with the driver. When you are sure or at least willing to pay to have someone help then call or e-mail and arrange to work with an engineer. We will work with you to determine the cause of the issue.

Support

The software described in this manual is provided at no cost to clients who have purchased the corresponding hardware. Minimal support is included along with the documentation. For help with integration into your project please contact sales@dyneng.com for a support contract. Several options are available. With a contract in place Dynamic Engineers can help with system debugging, special software development, or whatever you need to get going.

For Service Contact:

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