DYNAMIC ENGINEERING

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PCI2cPCI-XXX

User Manual Adapter for cPCI to PCI slot Models: -32, -32-IO, -64 bit PCI



cPCI-32 model shown

Key Features Plug and Play operation 32/64 bit PCI bus supported J2 IO connections supported on –IO version

> Manual Revision A1 Corresponding Hardware: Revision 01 Fab Number 10-2016-3001



PCI2cPCI-XXX

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This product has been designed to operate with cPCI Modules and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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FIGURE 1 IO PIN ASSIGNMENT

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Product Description

PCI2cPCI-32, PCI2cPCI-64, and PCI2cPCI-32-IO are related products used to adapt cPCI hardware into a PCI computer slot.

The first two models [-32 and -64] are for 32 and 64 bit cPCI models respectively. Both provide the PCI bus to the cPCI card installed. With the 32 bit model J1/P1 is supported. With the 64 bit model J1/P1 & J2/P2 are supported with J2/P2 covering the upper half of the PCI bus.

The -32-IO model has both connectors and J2/P2 covers the "rear IO" capability from the installed cPCI device. The cPCI IO connections are routed to two 50 pin headers [J1 & J2] and 4 additional bits on a 4 pin header J3. Suitable for carriers of PMC, IP models and standard rear IO cPCI-32 boards.

The connector table is best used as follows: determine which pin is used by the cPCI on J2 – this would mean looking at the cPCI design and [if present] the mezzanine and flowing through to the J2 connector. On the table find the pin on the header.

If you happen to use IP Modules the J1 and J2 connectors map directly into the rear IO specification for IP Modules. For PMC modules the IO will be spread across both J1 and J2 and potentially on J3 depending on the module.

Standard Ribbon cable and HDEterm50 can make an easy breakout for the rear IO.



IO Pin Assignment

Signal	Header Pin	cPCI Pin
A61	J3.1	P2.E1
A62	J3.2	P2.D1
A63	J3.3	P2.C1
A64	J3.4	P2.B1
IOA 1	J1.1	P2.A11
IOA 2	J1.2	P2.B11
IOA_3	J1.3	P2.C11
IOA_4	J1.4	P2.D11
IOA_5	J1.5	P2.E11
IOA_6	J1.6	P2.A10
IOA_7	J1.7	P2.B10
IOA_8	J1.8	P2.C10
IOA_9	J1.9	P2.D10
IOA_10	J1.10	P2.E10
IOA_11	J1.11	P2.A9
IOA_12	J1.12	P2.B9
IOA_13	J1.13	P2.C9
IOA_14	J1.14	P2.D9
IOA_15 IOA_16	J1.15 J1.16	P2.E9 P2.A8
IOA_10 IOA_17	J1.10 J1.17	P2.88
IOA_17 IOA_18	J1.18	P2.C8
IOA 19	J1.19	P2.D8
IOA_20	J1.20	P2.E8
IOA 21	J1.21	P2.A7
IOA_22	J1.22	P2.B7
IOA_23	J1.23	P2.C7
IOA_24	J1.24	P2.D7
IOA_25	J1.25	P2.E7
IOA_26	J1.26	P2.A6
IOA_27	J1.27	P2.B6
IOA_28	J1.28	P2.C6
IOA_29	J1.29	P2.D6
IOA_30	J1.30	P2.E6
IOA_31 IOA_32	J1.31 J1.32	P2.A5
IOA_32 IOA_33	J1.32 J1.33	P2.B5 P2.C5
IOA_33 IOA 34	J1.33 J1.34	P2.05 P2.D5
107_04	01.04	12.00



IOA_35 IOA_36 IOA_37 IOA_38 IOA_39 IOA_40 IOA_40 IOA_41 IOA_42 IOA_43 IOA_43 IOA_44 IOA_45 IOA_45 IOA_46 IOA_47 IOA_48 IOA_49 IOA_50	J1.35 J1.36 J1.37 J1.38 J1.39 J1.40 J1.41 J1.42 J1.43 J1.44 J1.45 J1.45 J1.46 J1.47 J1.48 J1.49 J1.50	P2.E5 P2.A4 P2.B4 P2.C4 P2.D4 P2.E4 P2.A3 P2.B3 P2.C3 P2.C3 P2.C3 P2.C3 P2.C3 P2.C2 P2.B2 P2.C2 P2.C2 P2.C2 P2.C2 P2.C2
IOB_1 IOB_2 IOB_3 IOB_4 IOB_5 IOB_6 IOB_7 IOB_7 IOB_8 IOB_9 IOB_10 IOB_11 IOB_12 IOB_13 IOB_14 IOB_15 IOB_16 IOB_17 IOB_18 IOB_19 IOB_20 IOB_21 IOB_22 IOB_23 IOB_24	J2.1 J2.2 J2.3 J2.4 J2.5 J2.6 J2.7 J2.8 J2.9 J2.10 J2.11 J2.12 J2.13 J2.14 J2.12 J2.13 J2.14 J2.15 J2.16 J2.17 J2.16 J2.17 J2.18 J2.10 J2.20 J2.21 J2.20 J2.21 J2.22 J2.23 J2.24	P2.A21 P2.B21 P2.C21 P2.D21 P2.E21 P2.A20 P2.B20 P2.C20 P2.C20 P2.C20 P2.C19 P2.C19 P2.C19 P2.C19 P2.C19 P2.C19 P2.C18 P2.A18 P2.C18 P2.C18 P2.C18 P2.C18 P2.C18 P2.C17 P2.C17 P2.C17 P2.C17



IOB_25 IOB_26 IOB_27	J2.25 J2.26 J2.27	P2.E17 P2.A16 P2.B16
IOB_28	J2.28	P2.C16
IOB_29	J2.29	P2.D16
IOB_30	J2.30	P2.E16
IOB_31	J2.31	P2.A15
IOB_32	J2.32	P2.B15
IOB_33	J2.33	P2.C15
IOB_34	J2.34	P2.D15
IOB_35	J2.35	P2.E15
IOB_36	J2.36	P2.A14
IOB_37	J2.37	P2.B14
IOB_38	J2.38	P2.C14
IOB_39	J2.39	P2.D14
IOB_40	J2.40	P2.E14
IOB_41	J2.41	P2.A13
IOB_42	J2.42	P2.B13
IOB_43	J2.43	P2.C13
IOB_44	J2.44	P2.D13
IOB_45	J2.45	P2.E13
IOB_46	J2.46	P2.A12
IOB_47	J2.47	P2.B12
IOB_48	J2.48	P2.C12
IOB_49	J2.49	P2.D12
IOB_50	J2.50	P2.E12

FIGURE 1

IO PIN ASSIGNMENT



Construction and Reliability

PCI2cPCI-XX is constructed out of 0.062 inch thick high temperature ROHS compliant FR4 material.

Through hole and surface mounting of components are used. High insertion and removal forces are required, which assists in the retention of components.

Thermal Considerations

PCI2cPCI-XX is a passive design with very low thermal dissipation. The installed cPCI card will not be in a standard cPCI chassis when using these adapters. Adequate cooling should be provided to enhance your development experience.



Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department Dynamic Engineering 150 DuBois St. Suite C Santa Cruz, CA 95060 831-457-8891 831-457-4793 fax support@dyneng.com



Specifications

Logic Interfaces:	PCI Interface 32/64 bit, universal signaling
Access types:	All PCI supported
CLK rates supported:	33/66 MHz. PCI
Software Interface:	NA
Access Modes:	Standard PCI accesses
Access Time:	Passive design with "no" delay added to accesses.
Interrupt:	INTA-D are supported
DMA:	REQ/GNT signals connected through
Onboard Options:	-32, -32-IO, -64
Interface:	-IO model has 2 x 50 pin Header Connectors plus 4 pin header for complete rear IO availability.
Dimensions:	Minimized board – PCI-32 or PCI-64 in width.
Construction:	High Temp ROHS compliant FR4 Multi-Layer Printed Circuit, Through Hole.
Power:	All rails connected through with mini-planes (+12, -12, 5, 3.3, VIO, Gnd).
User	NA
Other LED	NA.
Slots	NA
Temperature Range	-40C⇔+85C Components Standard
Temperature Coefficient:	2.17 W/ ^o C for uniform heat across adapter
MTBF	TBD



Order Information

Standard temperature range -40 PCI2cPCI-32	⇔85 ^ø C <u>http://www.dyneng.com/PCI2cPCI.html</u> 32 bit PCI adapter for cPCI
PCI2cPCI-32-IO	http://www.dyneng.com/PCI2cPCI.html 32 bit PCI adapter for cPCI with rear IO support
PCI2cPCI-64	http://www.dyneng.com/PCI2cPCI.html 64 bit PCI adapter for cPCI
HDRterm50	http://www.dyneng.com/HDRterm50.html 50-pin header to 50 screw terminal converter with DIN rail mounting.
HDRcabl50	50 pin ribbon cable compatible with PCI5IP and HDRterm50. Various lengths off-the-shelf, and custom

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