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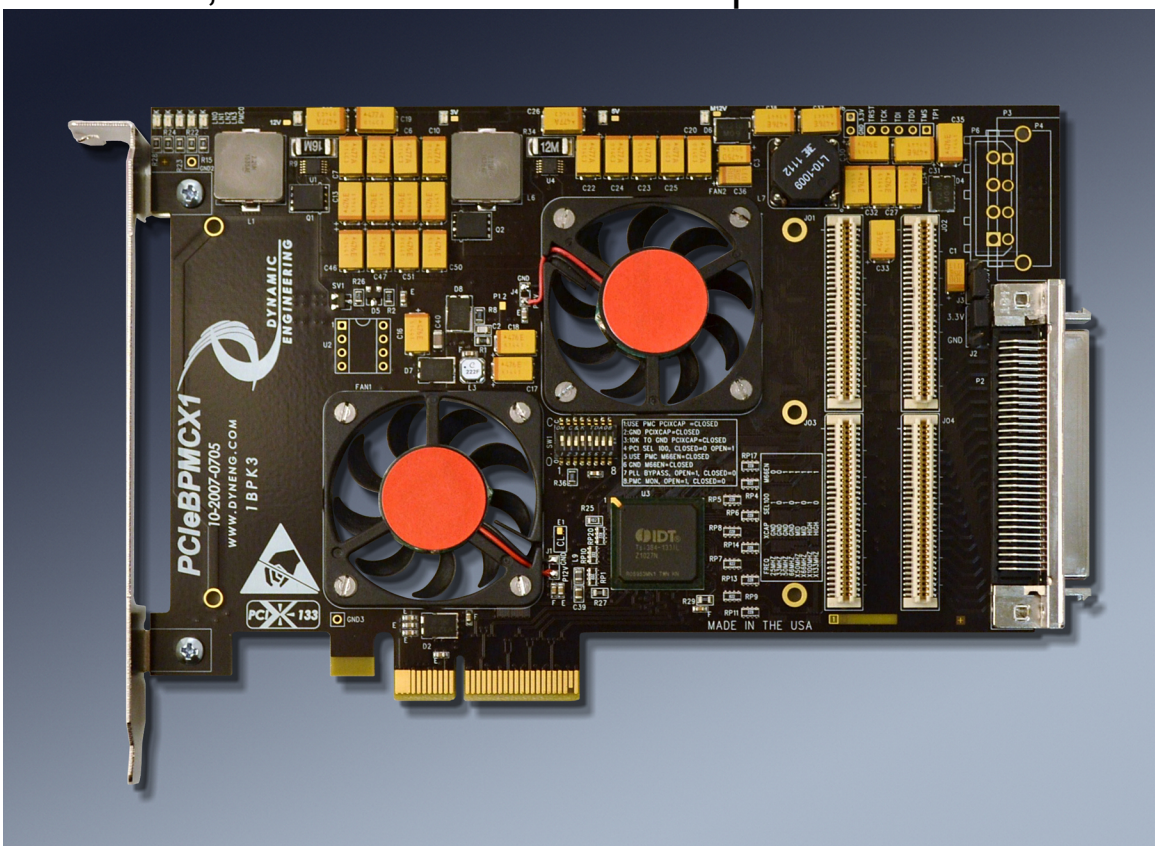
User Manual

PCIeBPMCX1- 4 PCIe Lane
PCIeBPMC – 1 PCIe Lane

PCI, PCI-X 1 Slot PMC Compatible Carrier



Revision F2
Corresponding Hardware: Revision A-K
Fab number:10-2007-070(1-11) for X1

PCIEBPMCX1
PCIeBPMC
PCIe, PCI and PMC Compatible Carrier

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Table of Contents

List of Figures

Product Description

PCIeBPMCX1 and PCIeBPMC are part of the Dynamic Engineering PCI Express and PMC Compatible family of modular I/O components. PCIeBPMCX1 and PCIeBPMC adapt a PMC to PCIe. The X1 was launched in 2007 and the single lane version in 2008. Thousands delivered.

The PMC, when mounted to PCIeBPMCX1 creates a stacked assembly which is PCI compliant height wise – only 1 slot used. The Bezel IO on the PMC, if any, is available at the standard PC IO port – typically at the rear of the computer. User IO on connector Pn4 is available for internal routing at the rear of the carrier card. A right angle SCSI connector is standard. Vertical connectors can be installed

PCIeBPMCX1 uses up to 4 PCIe lanes to operate with PCI-25, 33, 50, 66,100 or 133 speeds. PCIeBPMC utilizes 1 PCIe lane to operate with PCI-25, 33, 50, 66 speeds.

The 1 lane design can operate at any of the listed speeds. The 1 lane available may reduce the overall throughput depending on the application. Register accesses and other short bursted activity may not be affected. With longer DMA transfers at the higher bandwidth of the 4 lane version is recommended.

Many PC's are supplied with more 1 lane PCIe connectors than 4, 8 or 16 lane connectors. Many PMC's are 32/33 PCI implementations and can use the single PCIe lane slot without any reduction in speed compared to using in a four PCIe lane position.

Both designs are the same other than reducing the number of lanes connected, the mechanical size of the PCIe connector, tying the PRESENT signal to the 1 lane versus 4 lane operation for the two slots, and the number of LED's for PCIe lane status.

PCIeBPMCX1	4 lane min. backplane connector size	up to 4 lanes used
PCIeBPMC	1 lane min backplane connector size	1 lane used

With PCIeBPMCX1 => 4, 8, 16 or 32 lane connectors can be used. With PCIeBPMC any lane count connector can be used.

Unlike PCI, the PCIe specification provides for 12V power [only] to be used by

the Express module. A minimal amount of 3.3V is available from the Express connector but not enough to power typical PMC devices. Local power supplies operate from the +12V to create the rest of the PMC voltages [-12, 5V, 3.3V]. The 5V and 3.3V power supplies can source 9.5A each and the –12V is designed for 4A, but effectively limited by the single pin assigned by the PMC specification. For higher current requirement modules the **Zero Slot** FAN options are recommended.

The transparent bridge does not require any software interaction. Your PMC drivers will work without modification when hosted by the PCIeBPMC or PCIeBPMCX1. The bridge can provide higher bandwidth for DMA transfers if some settings are adjusted.

Special features:

- PCIe Compliant 1-4 lane design based on highest performance bridge TSI384.
- PCI, PCI-X compliant on secondary [PMC] bus
- LED on PMC Busmode "Present"
- LED's on plus 12V, minus 12V, plus 5V, plus 3.3V plus bridge power. Each is controlled by a voltage monitoring circuit. If illuminated the voltages are within tolerance.
- LED's on PCIe Lane Status (1,4)
- Local power supplies for +5, 3.3 and M12
  With revision J boards, the 5V and 3.3V supplies can be disabled, delayed, or instant on.
- VIO set to 3.3V.
- 32 or 64 bit operation
- 133, 100, 66, 50, 33 or 25 MHz operation.
- Front panel connector access through PCI bracket
- User IO [Pn4] available through SCSI II connector. Spare pins on SCSI connector can be shunt selected to power or ground. Routing done as matched length, differential pairs with 100 Ω differential impedance.
- Cooling cutouts for increased airflow to PMC's
- Optional Fan(s) for increased airflow, both positions have "zero slot" height feature
- Optional JTAG programming support
- Clearance for XMC connectors [rev 2 and later boards].
- User Selection for AC, DC and open for both PMC Bezel and PCIe Bezel.

The PCIeBPMCX1 is ready to use with the default settings. Just install the PMC onto the PCIeBPMCX1 and then into the system. There are a few settings to optimize performance.

Why the Tsi384 instead of the PEX8114? Most current PCIe carriers for PMC are using the PLX PEX8114 device. The Tundra Tsi384 has significantly better performance. For the details request the Tundra speed comparison document. It is a confidential document so we can't reprint the results here.

We can tell you that we ran more than 100K DMA loop-tests using the PMC BiSerial III MDS1 as a test bench. The DMA loop uses a message size (1Mb) significantly larger than the 1k x 32 FIFO within the FPGA. HW moves the data between FIFO's (TX to RX on each channel). DMA moves the data back again. The FIFOs are relatively small – compared to the file size being transferred. The TX and RX channels have independent DMA controllers (8) on the MDS1. The hardware starts transferring the RX side as soon as there is data in the RX FIFO.

The result is that data is being transferred in both directions using DMA across the PCIe bus. The transfers will be somewhat asynchronous to each other creating all possible conditions when allowed to run for an extended period of time.

The hardware ran for more than 54 hours without error. The test operates faster than in a standard PCI slot. When you do the math an impressive amount of data was transferred and checked. Even with Windows® the test sustained more than 4.6 Mb/s including error checking etc. With Linux or a real time OS the numbers would be much higher.

Faster, lower powered, simpler power supply requirements, higher MTBF. In short a better product. We use PLX devices on a number of our designs. In this case the Tundra part is superior.

DipSwitch Settings

Please note that the switch numbering and 'C' and 'O' definitions are per the silk screen.

The dipswitch is numbered SW1 and is located near the center of the board. SW1 controls the Bridge operation. UP = Closed and DOWN = Open.

For forced operation use the following settings: Note that the PMC must be capable of operating at the selected frequency. To truly force independent of the PMC open switch 1,5

Mode and Bus Rate	PCI_PCIXCAP	PCI_SEL100	PCI_M66EN
switches	**1,2,3**	**4**	**5,6**
PCI 25 MHz	C,C,C	O	C,C
PCI 33 MHz	C,C,C	C	C,C
PCI 50 MHz	C,C,C	O	C,O
PCI 66 MHz	C,C,C	C	C,O
PCI-X 50 MHz	C,O,C	O	C,O
PCI-X 66 MHz	C,O,C	C	C,O
PCI-X 100 MHz	C,O,O	O	C,O
PCI-X 133 MHz	C,O,O	C	C,O

For automatic operation use the following settings

Mode and Bus Rate	PCI_PCIXCAP	PCI_SEL100	PCI_M66EN
switches	**1,2,3**	**4**	**5,6**
Automatic selection	C,O,O	C/O	C,O

Please note that switch 4 is used to select between the upper and lower frequency at each frequency level (25/33, 50/66, 100/133)

Special selections for the Tsi Bridge
For more information please refer to the IDT[Tundra]® documentation

The DIPSWITCH has 8 switches. Normal IC pin numbering is used; 1-16 comprise switch 1, 2-15 => switch 2 and so forth.

Factory default is “C O O C C O O O” C= closed [up], O = Open [down].

Position 1 corresponds to S_PCIXCAP and P_PCIXCAP. When closed the signals are tied together. When open the signals are isolated. The S_PCIXCAP is tied to the PMC position PCIXCAP signal. P_PCIXCAP is tied to the Bridge. When connected together automatic operation is enabled; the PMC and Bridge negotiate for the frequency automatically. Setting to open isolates the two devices, and allows the user to override the PMC set-up.

DIPSWITCH pins 16, 15, and 14 are tied together to allow the user to control the bridge side of PCIXCAP with options on switches 1, 2, 3. Connecting the signals through on **switch 1** and leaving switches 2, 3 open is the default setting for standard operation.

Closing **switch 2** can be used to ground the Bridge side PCIXCAP signal and selectively ground the PMC version of the signal if position 1 is also closed. This has the effect of forcing the speed range to be 25-66 MHz.

Closing **switch 3** can be used to create an intermediate voltage on the PCIXCAP signal on the Bridge and optionally on the PMC side. There is a 56KΩ pull-up to 3.3 on the secondary side of the switch. Closing switch 3 adds the pull-down resistor – 10KΩ to ground. PMC's with PCI-X 66 capability should have the 10 KΩ pull-down on the PMC making the intermediate voltage selection automatic.

PMC cards operating at PCI 66 MHz [not PCI-X] will ground the PCIXCAP signal and leave M66EN high. The ground from the PMC will override the switch 3 setting unless switch 1 is open.

Switch 4 when open leaves PCI Select 100 pulled up to 3.3 though an 8.2KΩ resistor. If the switch is closed the signal is tied to ground. [feature added for revision 2 and later boards. Revision 1 boards can have this option added.] PCI Select 100 is used to toggle between 100 and 133 or 50 and 66 or 25 and 33. The default selection is closed to allow the PMC to select 33, 66, or 133 MHz.

Switch 5 and **Switch 6** correspond to S_M66EN and P_M66EN respectively. When Switch 5 is closed and Switch 6 is open the signals are connected together with a light pull-up on each side. This is the default setting. When Switch 6 is closed the Bridge side is forced to ground – low speed operation.

When open the signal is '1' assuming that the PMC does not pull the signal down. S_M66EN/P_M66EN acts as an open drain signal with any of the nodes capable of reducing the clock rate and all nodes required to operate at the higher

rate. Select the secondary side [PMC] PCI bus frequency. With the PCIe to PCI bridge the PCI clock is not related to the PCIe rate. The switches and card pin strapping control the frequency. Tying the M66EN between the bridge and PMC plus doing the same for the PCIXCAP signal will allow for automatic clock selection based on the PCI/PCI-X specifications.

Position 7 corresponds to PLL_BiPass. When closed the signal the PLL is bipassed. When open the PLL is engaged. Default is open for PLL operation.

Position 8 is used to ground the Monarch pin J2-64. A pull-up holds the signal high when the switch is not closed. Closing the switch grounds the signal.

Interrupts

Interrupts from the PMC are connected from the PMC to the primary PCIe bus. INTA through INTD are mapped indirectly to the bridge where the interrupt requests are mapped into PCIe control words and sent to the host computer. The host will respond over PCIe as programmed by the user software to deal with the interrupt. The operation is transparent to software as if the transaction happened over a PCI bus.

IDSEL

The IDSEL is set to AD20 for the PMC slot [secondary PCI].

PMC Interface miscellaneous notes:

Jn2 pins 58 and 64 are pulled up to VCC_IO with 4.7KΩ. Pin 60 is open. This configuration works with most Monarch capable PMC's. Please contact Dynamic Engineering if you need alternate settings. The monarch pin is also tied to the DIPSWITCH for user selection.

Options

PCIeBPMCX1 features cooling cutouts designed to support the addition of a fan in one and/or two positions for the PMC. On PrPMC's, and other PMC's with high thermal loads the fan option is a good idea. On cards with a lower thermal profile the fan(s) is not needed. The fan produces ~4.7 CFM in a small area to create a high LFM rating suitable for most cooling requirements. The fan used has a relatively low noise rating for quiet operation. Position 1 is closest to the PCI bezel and position 2 is closer to the PMC connectors.

The fan positions are designed to allow the fan to be mounted through the PCB. The thickness of the PCB is used to reduce the overall thickness of the fan. By doing so fans can be used, and be legal for height [less than .105"] on the rear of the card. Both Fan positions are located outside of the connector area to allow the PMC the full height [4.7 mm] per the PMC specification plus some air gap.

Please note that the full 10 MM is available within the entire connector area, fans or not.

Options include –FAN1, -FAN2, -FAN12, -FAN1R, -FAN1R2, -FAN1R2R -1 is the slot closest to the bezel. –2 is the position closest to the PMC connectors. R designates rear mounting. No "R" indicates "zero slot" fan installation. The rear mounted fans have higher air flow with ~8 CFM per fan.

Power supplies

PCIe has one glaring weakness… not enough power to the main PCIe connector for the smaller lane count boards. 12V, 3.3V, and 3.3V AUX are available on the backplane connector. PCIeBPMCX1 uses the 12V and 3.3V AUX. The 3.3V rail is used for the bridge and not connected to the PMC. The PCIe 12V is also used to generate the 1.2V for the Bridge.

12V is Diode coupled to a second power connector located at the rear of the card. For applications requiring more than ~60W total power consumption the rear connector should be added.

The 12V rail is tied to PMC 12V input and to the power supplies that generate the M12, 5V, 3.3V.

The 12V input rail at the gold finger connector is limited to about 5.5A max. 66W is the maximum input power. The power supplies have been measured to be about 90% efficient leaving 59.4W for internal use. The Tsi384 can use up to 2W leaving a minimum of 57.4W for the PMC.

The 5V and 3.3V supplies can generate 9.5A each – exceeding the capacity of the 12V input rail. Minus 12 has excess capacity and should be limited to 1A due to pin limitations on the PMC connector. +12V also shares this limitation.

For designs using less than 5A on the 5V and 3.3V rails and operating in a “lab” environment no additional cooling is required. With loads approaching 5A and or operating at higher temperatures forced air cooling is required. The zero slot fans provide enough air flow to extend the operational limit of the supplies. The full 9.5A may require additional airflow to the rear of the card depending on the operational temperature etc.

For revision 3 and later boards the FET’s have been moved to the front of the card and changed to a different package with the Drain tied to a pad on the bottom of the part allowing direct thermal contact. The improved package reduces the thermal resistance sufficiently to move the max no air flow current rating. In addition the inductor and FET have improved characteristics allowing for a max of 9.5A.

3.3 AUX is directly routed to the PMC on the 3.3V AUX pin.

Many implementations will stay within the 57.4W limitation. For those designs needing the **extra** power; there are two basic options. Select the “OT” connector for screw terminal type connection, and select the ‘DD” options to mate with the internal PC power supply wiring harness.

Three connector options are available for revision 2 boards and later. –DD for a “Disk Drive” style right angle connector that will mate with the standard 4 pin HDD cable. Each pin can handle 5A. There is 1 12V pin on this style connector allowing an additional 60W to be input to the board. The –DDV is a vertical version of the –DD connector and can be used when needed in a 1/2 length configuration.

The –OT version has a screw terminal block connection on the cable side. This connector has 2 high current pins for +12 and 2 for ground allowing higher current input than the –DD and –DDV version as well as larger wire and flexibility if making your own cable to a custom supply.

With revision J [X1] and E[1 lane] two addional headers are added to the design. **J1** controls the 3.3V supply and **J4** controls the 5V supply. With no shunt installed the power supplies are disabled. If your PMC does not use the 3.3V or 5V power it is recommended to remove the corresponding shunt. Please note: the corresponding LED will go dark since the power is out of tolerance in this configuration. When 1-2 are connected the power supply is enabled with a delayed start-up. When 2-3 are connected the power supply is enabled without a delay.

The headers are labeled in the silk-screen. The square pad is pin 1 if you need a second indicator.

The delay waits for the +12 to reach approximately 5V before starting a supervisor circuit timer. The circuit adds an additional delay before enabling the power supply. The delay can reduce the system in-rush requirement. Please note: in some systems the enumeration happens early and the installed PMC may need the instant on setting to be configured in time to be enumerated correctly.

You can see the affect by delaying one supply and not the other, powering on and looking at the monitor LED’s.

P3, P4, P6 Pinout

NAME	P3	P4	P6
GND	1,2	2,3	2,3
+12	3,4	1	1
+5	NA	4	4

Please note that the 5V power on P4 and P6 is not used by the PCIeBPMCX1.

P4 = -DD option right angle mount Disk Drive style connector to mate with standard PC HDD power cable

P6 = -DDV option vertical mount Disk Drive style connector to mate with standard PC HDD power cable

P4 = -OT option high current connector. Mate supplied when this option is selected.

J8, J9 Pinout

J8 and J9 are used to select the grounding option for the PCIe and PMC Bezel's respectively. The silk-screen shows AC and DC positions for a shunt to select AC = .1 uF cap to ground , DC = direct connection to ground. No shunt = open connection to ground.

Frequently it is best to DC couple on one side and AC on the other side of a common cable to provide a reference for the cable shield and prevent ground loops.

J2, J3 Pinout

J2 and J3 are three pin headers used to select the definition of pins 33,67(J2) and 34,68(J3) on the SCSI connector. The headers are installed if the –SCSI option is selected when ordering. Shunting pins 1-2 applies 3.3V, 2-3 applies ground. The silk-screen shows 3.3 and GND positions for a shunt to select No shunt = open connection. The pins and shunts can handle just under 1A per header. Not fuse protected.

PMC Module Backplane IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface – from Pn4 to the PCIeBPMCX1 connectors. Also see the User Manual for your PMC board for more information.

SCSI II [P2]		Pn4	
35	36	1	2
1	2	3	4
37	38	5	6
3	4	7	8
39	40	9	10
5	6	11	12
41	42	13	14
7	8	15	16
43	44	17	18
9	10	19	20
45	46	21	22
11	12	23	24
47	48	25	26
13	14	27	28
49	50	29	30
15	16	31	32
51	52	33	34
17	18	35	36
53	54	37	38
19	20	39	40
55	56	41	42
21	22	43	44
57	58	45	46
23	24	47	48
59	60	49	50
25	26	51	52
61	62	53	54
27	28	55	56
63	64	57	58
29	30	59	60
65	66	61	62
31	32	63	64
33	67	Open, +3.3 or GND via J2 silk screen defined	
34	68	Open, +3.3 or GND via J3	

FIGURE 1 PCIEBPMCX1 PN4 INTERFACE STANDARD

Read table:
P2-1 = Pn4-3
P2-35 = Pn4-1
etc.
Signals are matched length and differentially routed with 100 ohm impendance.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
The PMC is mounted to the PCIeBPMCX1 prior to installation within the chassis. For best results: with the PCI bracket installed, install the PMC at an angle so that the PMC front panel bezel penetrates the PCI bracket then rotate down to mate with the PMC [PnX] connectors.

There are four mounting locations per PMC. Two into the PMC mounting bezel, and two for the standoffs near the PMC bus connectors.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId for the PMC installed and an interrupt level. If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. The device manager can be used for Windows OS installations.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCIeBPMCX1 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the PMC's installed onto the PCIeBPMCX1 than the PCIEBPMCX1 itself, and it is smart system design when it can be achieved.

Construction and Reliability

The PCIeBPMCX1 is constructed out of 0.062 inch thick High Temp FR4 ROHS compliant material. Cooling cutouts have been designed into the product for improved airflow to the PMC sites. The components on the PCIeBPMCX1 are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in the situation where a large portion of the board has little or no power dissipation.

Surface mounted components are used. The connectors are SMT for the PMC bus and through hole for the IO.

The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC Module is secured against the carrier with the PMC connectors. It is recommended, for enhanced security against vibration, that the PMC mounting screws are installed. The screws are supplied with the PMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels and other PMC hardware available at a reasonable cost if your PMC was not shipped with some of the required attachment hardware or if it has been misplaced.

Thermal Considerations

If the PMC installed has large heat dissipation; forced air cooling is recommended.

A fan option is available for high thermal load PMC's or for a chassis with a lack of air circulation. The fan option is required for PMC's using 5A or more on either or both of the 5V or 3.3V rails.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

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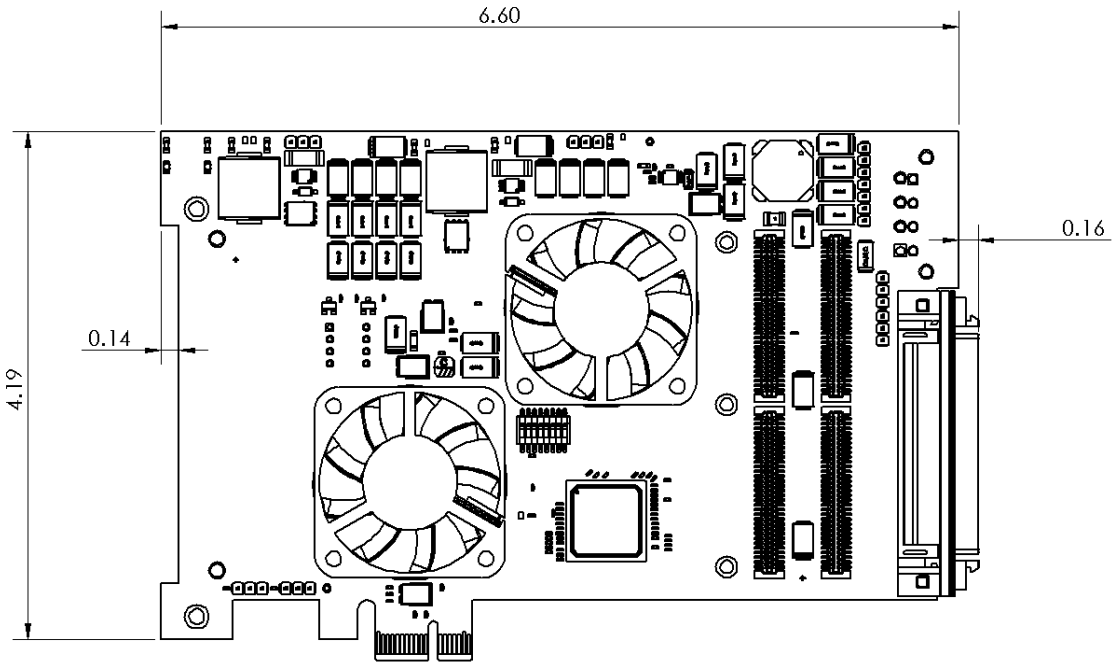
Board Outline Drawing



PCIeBPMC Top View Dimensions

Revision 05 single lane version shown.

Specifications

Logic Interfaces:	PMC: PCI, PCI-X Interface PCIe: 1-4 lanes
Access types:	PCI bus accesses
CLK rates supported:	133, 100, 66, 50, 33, 25 MHz PCI(x) clock rates
Bus Size Supported:	32 or 64 bit wide operation
Software Interface:	Transparent Bridge. Tsi384 registers in configuration space. Access to registers is usually not required
Initialization:	Dipswitch settings for optimized performance, factory defaults usually best choice, no software required to operate transparent bridge.
Interface:	PMC front bezel via PCI bracket and User IO connector via SCSI II connector
Dimensions:	1/2 length PCIe board, single PCIe slot width with PMC installed
Construction:	High Temp ROHS compliant FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.

Order Information

standard temperature range **–40 - 85ºC** rated components

PCIeBPMCX1	4 PCIe lane connector. 1-4 lane operation. Compatible with 4 or more lane backplane connectors. http://www.dyneng.com/pciebpmcx1.html
PCIeBPMC	1 PCIe lane connector, 1 lane operation. Compatible with 1 or more lane backplane connectors http://www.dyneng.com/pciebpmc.html
	Common Features 1/2 length PCIe adapter with PMC positions Options include: –FAN1, -FAN2, -FAN12, -FAN1R, -FAN1R2 1 is the slot closest to the bezel. –2 is the position closest to the PMC connectors. R designates rear mounting. No "R" indicates "**zero slot**" fan installation. -**NC** [SCSI connector not installed] -**SV** vertical [SCSI connector installed] -**ROHS** for ROHS compliant processing -**CC** for conformal coating option -**DD** for disk drive added power connector -**DDV** for vertical disk drive added power conn. -**OT** for high power added power connector
HDEterm68	http://www.dyneng.com/HDEterm68.html 68 pin SCSI II to 68 screw terminal converter with DIN rail mounting.
HDEcabl68	http://www.dyneng.com/HDEcabl68.html 68 pin SCSI cable available in several lengths.