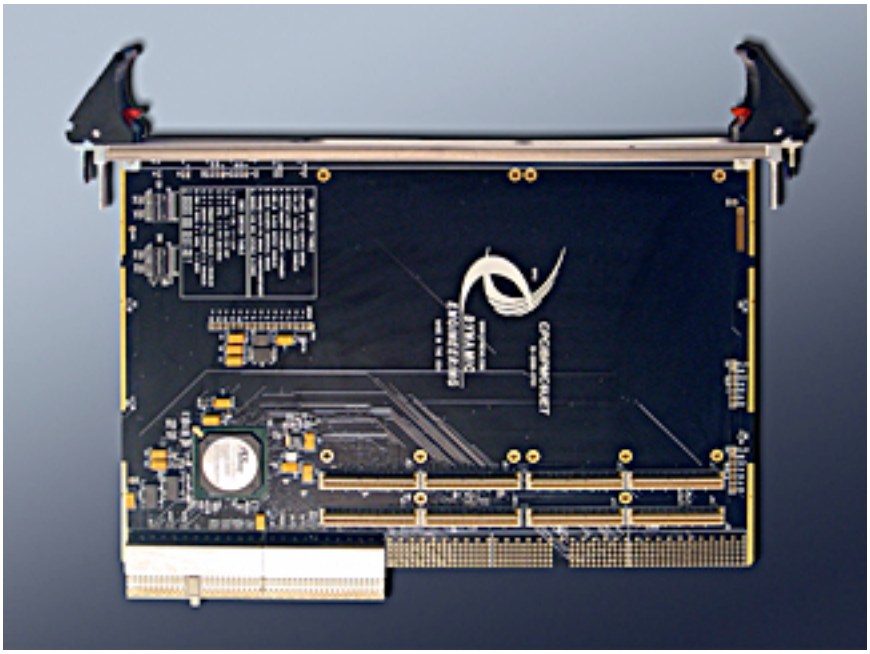
DYNAMIC ENGINEERING
150 DuBois St. Suite C Santa Cruz CA 95060
831-457-8891 **Fax** 831-457-4793
http://www.dyneng.com
sales@dyneng.com
Est. 1988

User Manual

cPCIBPMC6UET

cPCI 6U 4HP 2 Slot PMC Compatible Carrier
Extended Temperature



Revision D
Corresponding Hardware: Revision D
Fab number10-2006-0704

cPCIBPMC6UET
cPCI and PMC Compatible Carrier

Dynamic Engineering
150 DuBois St Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 FAX

Manual Revision D. Revised 12/09/2009

Table of Contents

List of Figures

Product Description

cPCIBPMC6UET is part of the Dynamic Engineering cPCI and PMC compatible family of modular I/O components.

The cPCIBPMC6UET is a 6U 4HP design with two PMC positions. The design is rated for industrial temperature operation “ET” –40C ⇔ +85C.

The bridge isolates the cPCI PCI bus from the local PMC PCI bus allowing mixed frequency and width operation. VIO is programmable allowing mixed voltage definitions as well.

Easy to use as a plug and play device. In transparent mode no special software is required for the carrier. A special hidden address range is available to allow high-speed local bus operations without interfering with the cPCI bus.

Special features:

- Universal cPCI 6U 4HP.
- Extended temperature range [-40 +85C]

LED names within quotes:

- LEDs on PMC Busmode “PMC-0” “PMC-1”
- LED on plus 12V “P12V”
- LED on minus 12V “M12V”
- LED on plus 5V “P5V”
- LED on plus 3.3V “P3.3V”
- LED on 1.8V “P1.8V”
- User selectable secondary VIO.
- 32 or 64 bit operation on either bus
- 66 or 33 MHz operation. With 66 MHz. primary bus speed the secondary bus can be 66 or 33 MHz. Secondary bus can be at a higher rate than the primary bus using oscillator option.
- Front panel connector access through cPCI bracket
- Rear Panel IO support with –RP model
- JTAG programming support option
- GPIO bus option

The cPCIBPMC6UET is ready to use with the default settings. Just install the PMC’s onto the cPCIBPMC6UET and then into the system. There are a few settings to optimize performance.

DipSwitch Settings

Please note that the switch numbering and '1' and '0' definitions are per the silk screen.

Quick reference:
Set the dip switch 1 :"00110001" for 32 bit operation Default (1—8)
Set the dip switch 2 :"11011111" for the x32/33 Default (1—8)

Set the dip switch 1 :"00010001" for the x64 operation (1—8)
Set the dip switch 2 :"11000111" for the x64/66 (1—8)

DIPSWITCH #1 [SW1 table on silk-screen]
Select the "green power" clock setting. With the new revision of the bridge [PLX 6466] the secondary clock can be set to be driven low or continue to operate when in the power down state. With the **DIP switch 1** set to '1' the clock will be driven low during power down, and with the switch '0' the clock will always be driven. The factory setting is '0'. **BPCC_EN** is the signal controlled with switch 1.

Select the Bridge "S_CLKOFF". The bridge can drive or not drive the CLK outputs. With a standard PMC installed the clocks should be enabled. With **switch #2** set to '0' the clocks are enabled, with the switch in position '1' the clocks are disabled. **CLK_OFF** is the signal controlled with switch number 2. The factory setting is '0'.

Select the Bridge "DEV64#". The bridge can accommodate 32 and 64 bit cards installed into the PMC slot. With **switch #3** set to '1' the bridge will read the installed PMC to be 32 bit. With the switch set to '0' the bridge will report a 64 bit device. The factory setting is '1'. Please note that the hardware will detect the ACK64# signal to determine the port width for transactions.

PBOOT is selected with **Switch #4**. When '0' the secondary port is selected for "Boot Priority". When '1' the primary port is selected. The PBOOT setting has meaning when in the non-transparent modes. The factory setting is '1'.

MSK_IN is selected with **Switch #5**. When '0' the Bridge clock outputs are enabled. When '1'' the bridge clock outputs are disabled. Both Mask and Clock Off need to be enabled for normal operation. The factory setting is '0'.

UMODE is selected with **Switch #6**. When '1' and in non-transparent mode the bridge will be configured to be a "universal bridge". The factory setting is '0'.

TRANS# is selected with **Switch #7**. When '0' the bridge will act in transparent mode. When '1' the bridge will be in non-transparent mode. The factory setting is '0'.

Select the secondary side [PMC] PCI bus frequency. The options are to use the PCI bus speed [primary] or to force 33 MHz on the secondary side. The PMC to be installed must be 66 MHz compliant to use the 66 MHz secondary side option. The speed is controlled with the **DIP switch #8** position. '1' = 66 MHz capable secondary side. '0' = 33 MHz. **SM66EN** is the signal name controlled by the switch. The factory setting is '0'.

The SM66EN signal is also routed to the PMC connector pin M66EN. If the PMC uses the M66EN as an input then the dipswitch can be used to control the frequency. If the PMC uses the M66EN pin as a control, then the Switch may have no effect. For example if the switch is in the '1' position and the PMC is selecting M66EN = '0' then the PMC will "win" and the signal will be at the 33 MHz setting. Both the dipswitch and the PMC M66EN have to be enabled for 66 MHz.

Please note that the secondary side can operate at frequencies other than the PCI frequency by using the oscillator. For example the PCI speed can be 33 and the secondary side be 66 if the oscillator is used. The Bridge takes care of the rate matching and has large FIFO's. Please refer to the DIPSwitch #2 definitions.

DIPSWITCH #2 [SW2 table on silk-screen]

Switch #1 selects the secondary side VIO [**SVIO**]. When the switch = '1' 3.3V is selected for the secondary side. When '0' is selected 5V is the VIO definition. The VIO plane is a reference for the IO level. The specification does not prohibit larger current consumption from these pins. The cPCIBPMC6UET design utilizes a MOSFET to control the 5V or 3.3V rails onto the VIO plane. Max consumption on the VIO rail is 3A. The factory setting is '1'.

Switch #2 selects the clock reference to use for the secondary side. "1' selects the PCI clock from the primary side and '0' selects the installed oscillator. The oscillator has a default frequency of 66 MHz. Please note that the secondary side frequency still depends on the M66EN definition – the bridge will divide the clock if set to 33 capable. The factory setting is '1'.

Switch #3 selects the addressing mode. When '1' the Private memory space is selected for the secondary side, when '0' the standard memory map is selected. The factory setting is '0'. **PRVDEV/XBMEM** is the signal controlled by this switch. It is recommended to read the PLX manual on the 64/66 when this signal is to be used.

Switch #4 selects **Primary PLL** enabled or not. '1' disables the PLL and '0' enables the PLL. The factory setting is '1'. If operating at 50 MHz or more on the primary side the PLL should be enabled. When operating below 50 MHz the PLL should not be enabled. At 33 MHz disable. At 66 MHz enable.

Switch #5 selects **Secondary PLL** enabled or not. '1' disables the PLL and '0' enables the PLL. The factory setting is '1'. If operating at 50 MHz or more on the secondary side the PLL should be enabled. When operating below 50 MHz the PLL should not be enabled. At 33 MHz disable. At 66 MHz enable.

Switch #6 selects **PMC IDSEL** range. '0' selects the lower range with AD16 and AD17 used for slots 0 and 1 respectively. '1' selects the upper range with AD20 and AD21 The factory setting is '1'.

Switch #7 selects **PMC Monarch Mode position 0**. For PrPMC's using the Monarch Mode pin, closing the switch ['0'] will cause the Monarch Pin [64] at the PMC to be tied through a 1KΩ resistor to ground. With the switch open the Monarch pin is tied to 3.3V through 4.7KΩ. The factory setting is '1'.

Switch #8 selects **PMC Monarch Mode position 1**. For PrPMC's using the Monarch Mode pin, closing the switch ['0'] will cause the Monarch Pin [64] at the PMC to be tied

through a 1KΩ resistor to ground. With the switch open the Monarch pin is tied to 3.3V through 4.7KΩ. The factory setting is '1'.

Interrupts

Interrupts from the PMC's are connected from the PMC to the primary PCI bus. INTA through INTD are mapped directly to the primary bus segment for position 0 and are rotated to connect [PMC] B,C,D,A to [PCI] A,B,C,D for slot 1.

Options

Dynamic Engineering offers two versions of the cPCIBPMC6UET design.

The base design supports PMC's with IO through the bezel.

The –RP version adds the J3 and J5 connectors to add "Rear Panel" IO capabilities. J4 has a position, and is not installed. If you want J4 installed please contact Dynamic Engineering.

For designers using the –RP version of the card the Dual PIM Carrier [http://www.dyneng.com/pim_carrier.shtml] has compatible IO definitions and provides an easy way to connect rear panel cabling. Custom and off-the-shelf PIMs [PMC IO Modules] are available. For larger quantities Dynamic Engineering can "flatten" the carrier/PIM combination into a custom IO card.

Other Signals

PME is tied between the cPCI connector and the PMC positions bypassing the bridge as a standard setting. The bridge can be inserted into the path if desired. Resistor jumpers are used for this option. Please contact Dynamic Engineering for this option.

Reset Out on PMC position 0 is tied to Reset In on the secondary side of the bridge. The signal is pulled-up for non-PrPMC implementations. This connection will allow the PrPMC to cause a reset to the local side of the bridge. More details are available in the PLX 6466 data book.

JTAG support is available for each slot independently. The JTAG header positions are clearly marked in the silk screen. The headers are frequently not used and are not installed unless requested. Please contact Dynamic Engineering for this option.

The Bridge supports a GPIO function. A header position is available with the positions clearly marked in the silk-screen. The header is installed by request. Please contact Dynamic Engineering for this option. The lower 4 bits are terminated with 4.7KΩ to 3.3V. The upper bits have internal [bridge] pull-ups.

PMC Slot 0 Rear Panel IO Interface Pin Assignment

Slot 0 PMC	J3	PIM connection if Dual Carrier utilized
PMC_0_IO1	J3.E13	J14.1
PMC_0_IO2	J3.D13	J14.2
PMC_0_IO3	J3.C13	J14.3
PMC_0_IO4	J3.B13	J14.4
PMC_0_IO5	J3.A13	J14.5
PMC_0_IO6	J3.E12	J14.6
PMC_0_IO7	J3.D12	J14.7
PMC_0_IO8	J3.C12	J14.8
PMC_0_IO9	J3.B12	J14.9
PMC_0_IO10	J3.A12	J14.10
PMC_0_IO11	J3.E11	J14.11
PMC_0_IO12	J3.D11	J14.12
PMC_0_IO13	J3.C11	J14.13
PMC_0_IO14	J3.B11	J14.14
PMC_0_IO15	J3.A11	J14.15
PMC_0_IO16	J3.E10	J14.16
PMC_0_IO17	J3.D10	J14.17
PMC_0_IO18	J3.C10	J14.18
PMC_0_IO19	J3.B10	J14.19
PMC_0_IO20	J3.A10	J14.20
PMC_0_IO21	J3.E9	J14.21
PMC_0_IO22	J3.D9	J14.22
PMC_0_IO23	J3.C9	J14.23
PMC_0_IO24	J3.B9	J14.24
PMC_0_IO25	J3.A9	J14.25
PMC_0_IO26	J3.E8	J14.26
PMC_0_IO27	J3.D8	J14.27
PMC_0_IO28	J3.C8	J14.28
PMC_0_IO29	J3.B8	J14.29
PMC_0_IO30	J3.A8	J14.30
PMC_0_IO31	J3.E7	J14.31
PMC_0_IO32	J3.D7	J14.32
PMC_0_IO33	J3.C7	J14.33
PMC_0_IO34	J3.B7	J14.34
PMC_0_IO35	J3.A7	J14.35
PMC_0_IO36	J3.E6	J14.36
PMC_0_IO37	J3.D6	J14.37
PMC_0_IO38	J3.C6	J14.38
PMC_0_IO39	J3.B6	J14.39
PMC_0_IO40	J3.A6	J14.40
PMC_0_IO41	J3.E5	J14.41
PMC_0_IO42	J3.D5	J14.42
PMC_0_IO43	J3.C5	J14.43
PMC_0_IO44	J3.B5	J14.44
PMC_0_IO45	J3.A5	J14.45
PMC_0_IO46	J3.E4	J14.46
PMC_0_IO47	J3.D4	J14.47
PMC_0_IO48	J3.C4	J14.48
PMC_0_IO49	J3.B4	J14.49
PMC_0_IO50	J3.A4	J14.50
PMC_0_IO51	J3.E3	J14.51
PMC_0_IO52	J3.D3	J14.52
PMC_0_IO53	J3.C3	J14.53
PMC_0_IO54	J3.B3	J14.54
PMC_0_IO55	J3.A3	J14.55
PMC_0_IO56	J3.E2	J14.56
PMC_0_IO57	J3.D2	J14.57
PMC_0_IO58	J3.C2	J14.58
PMC_0_IO59	J3.B2	J14.59
PMC_0_IO60	J3.A2	J14.60
PMC_0_IO61	J3.E1	J14.61
PMC_0_IO62	J3.D1	J14.62
PMC_0_IO63	J3.C1	J14.63
PMC_0_IO64	J3.B1	J14.64

FIGURE 1 CPCIBPMC6UET POSITION O PN4 INTERFACE STANDARD

In the table above Slot 0 PMC and J3 are part of the cPCIBPMC6UET design. The third column [blue] for the PIM is shown as a reference for designers utilizing rear panel IO. The PIM markings are not found on the cPCIBPMC6UET card. The cPCI Dual PIM carrier is designed to match the cPCIBPMC6UET and provide the two PIM positions.

PMC Slot 1 Rear Panel IO Interface Pin Assignment

Slot 1 PMC	J5	PIM connection if Dual Carrier utilized
PMC_1_IO1	J5.E13	J24.1
PMC_1_IO2	J5.D13	J24.2
PMC_1_IO3	J5.C13	J24.3
PMC_1_IO4	J5.B13	J24.4
PMC_1_IO5	J5.A13	J24.5
PMC_1_IO6	J5.E12	J24.6
PMC_1_IO7	J5.D12	J24.7
PMC_1_IO8	J5.C12	J24.8
PMC_1_IO9	J5.B12	J24.9
PMC_1_IO10	J5.A12	J24.10
PMC_1_IO11	J5.E11	J24.11
PMC_1_IO12	J5.D11	J24.12
PMC_1_IO13	J5.C11	J24.13
PMC_1_IO14	J5.B11	J24.14
PMC_1_IO15	J5.A11	J24.15
PMC_1_IO16	J5.E10	J24.16
PMC_1_IO17	J5.D10	J24.17
PMC_1_IO18	J5.C10	J24.18
PMC_1_IO19	J5.B10	J24.19
PMC_1_IO20	J5.A10	J24.20
PMC_1_IO21	J5.E9	J24.21
PMC_1_IO22	J5.D9	J24.22
PMC_1_IO23	J5.C9	J24.23
PMC_1_IO24	J5.B9	J24.24
PMC_1_IO25	J5.A9	J24.25
PMC_1_IO26	J5.E8	J24.26
PMC_1_IO27	J5.D8	J24.27
PMC_1_IO28	J5.C8	J24.28
PMC_1_IO29	J5.B8	J24.29
PMC_1_IO30	J5.A8	J24.30
PMC_1_IO31	J5.E7	J24.31
PMC_1_IO32	J5.D7	J24.32
PMC_1_IO33	J5.C7	J24.33
PMC_1_IO34	J5.B7	J24.34
PMC_1_IO35	J5.A7	J24.35
PMC_1_IO36	J5.E6	J24.36
PMC_1_IO37	J5.D6	J24.37
PMC_1_IO38	J5.C6	J24.38
PMC_1_IO39	J5.B6	J24.39
PMC_1_IO40	J5.A6	J24.40
PMC_1_IO41	J5.E5	J24.41
PMC_1_IO42	J5.D5	J24.42
PMC_1_IO43	J5.C5	J24.43
PMC_1_IO44	J5.B5	J24.44
PMC_1_IO45	J5.A5	J24.45
PMC_1_IO46	J5.E4	J24.46
PMC_1_IO47	J5.D4	J24.47
PMC_1_IO48	J5.C4	J24.48
PMC_1_IO49	J5.B4	J24.49
PMC_1_IO50	J5.A4	J24.50
PMC_1_IO51	J5.E3	J24.51
PMC_1_IO52	J5.D3	J24.52
PMC_1_IO53	J5.C3	J24.53
PMC_1_IO54	J5.B3	J24.54
PMC_1_IO55	J5.A3	J24.55
PMC_1_IO56	J5.E2	J24.56
PMC_1_IO57	J5.D2	J24.57
PMC_1_IO58	J5.C2	J24.58
PMC_1_IO59	J5.B2	J24.59
PMC_1_IO60	J5.A2	J24.60
PMC_1_IO61	J5.E1	J24.61
PMC_1_IO62	J5.D1	J24.62
PMC_1_IO63	J5.C1	J24.63
PMC_1_IO64	J5.B1	J24.64

FIGURE 2 CPCIBPMC6UET POSITION 1 PN4 INTERFACE STANDARD

In the table above Slot 1 PMC and J5 are part of the cPCIBPMC6UET design. The third column [blue] for the PIM is shown as a reference for designers utilizing rear panel IO. The PIM markings are not found on the cPCIBPMC6UET card. The cPCI Dual PIM carrier is designed to match the cPCIBPMC6UET and provide the two PIM positions.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
The PMC is mounted to the cPCIBPMC6UET prior to installation within the chassis. For best results: with the cPCI bracket installed, install the PMC at an angle so that the PMC front panel bezel penetrates the cPCI bracket then rotate down to mate with the PMC [PnX] connectors.

There are four mounting locations per PMC. Two into the PMC mounting bezel, and two for the standoffs near the PMC bus connectors.

Start-up
A third party PCI device cataloging tool will be helpful to check that the VendorID and CardID are “seen” by the OS.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCIBPMC6UET when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the PMC installed into the cPCIBPMC6UET than the cPCIBPMC6UET itself, and it is smart system design when it can be achieved.

Construction and Reliability

The cPCIBPMC6UET is constructed out of 0.062 high temp ROHS compliant material. Gold has been used for plating rather than Tin for improved performance over time. “leaded or unleaded” components can be used along with solder choices. Dynamic Engineering can support both processes.

Surface mounted components are used. The connectors are SMT for the PMC bus and through hole [compression fit] for the cPCI. The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC Modules are secured against the carrier with the PMC connectors. It is recommended, for enhanced security against vibration, that the PMC’s mounting screws are installed. The screws are supplied with the PMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels and other PMC hardware available at a reasonable cost if your PMC was not shipped with some of the required attachment hardware or if it has been misplaced.

Thermal Considerations

If the PMC’s installed have a large heat dissipation; forced air cooling is recommended.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $125. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
InterNet Address support@dyneng.com

Specifications

Logic Interfaces:	PCI Interface 33/32 ⇔ 66/64
Access types:	PCI bus accesses
CLK rates supported:	33 or 66 MHz PCI clock rates
Software Interface:	transparent Bridge. PLX6466 registers in configuration space
Initialization:	Selections for VIO, primary and secondary clock rates
Interface:	PMC front bezel via cPCI bracket. Rear Panel IO option.
Dimensions:	6U 4HP
Construction:	High Temp ROHS compliant Multi-Layer Printed Circuit board, Through Hole and Surface Mount Components. Add –ROHS for ROHS processing.

Order Information

standard temperature range –40 ⇔ +85ºC

cPCIBPMC6UET	6U 4HP cPCI card with two PMC positions http://www.dyneng.com/cPCIBPMC6UET.html
cPCIBPMC6UET-RP	6U 4HP cPCI card with wo PMC positions and RP IO connections on J3 / J5 http://www.dyneng.com/cPCIBPMC6UET.html
-CC	Conformal Coating is available as an option.
-ROHS	Add for ROHS processing.
Rear Panel IO support	Dual PIM carrier [6U] Two PIM positions with compatible IO definitions for J3/J5 http://www.dyneng.com/pim_carrier.shtml