

# **DYNAMIC ENGINEERING**

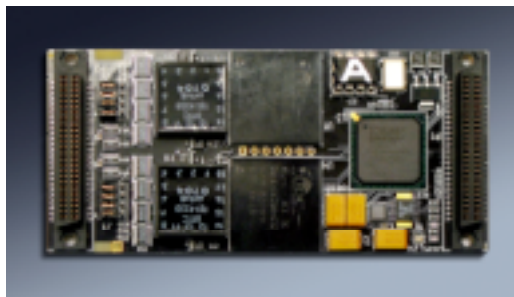
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Est. 1988

## **User Manual**

# **IP-1553**

**MIL-STD-1553 Interface  
1 or 2 Dual Redundant channels  
direct or transformer coupled**

**IndustryPack® Module**



Revision A2  
Corresponding Hardware: Revision A  
PROM revision B1  
10-2006-1401

**IP-1553**  
**MIL-STD-1553 Interface**  
**IndustryPack® Module**

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## Product Description

IP-1553 is part of the IndustryPack® “IP” Module family of modular I/O components by Dynamic Engineering. The IP-1553 provides two independent 1553 controllers each with redundancy. The ACE BU64863 interface provides the protocol processing and integrated transceivers. A transformer with multiple taps provides the Direct or Transformer coupled capability. IP-1553 can be selectively built with one or two 1553 controllers. Please add the correct suffix to select the model you require. (-1,-2)

The ACE supports programmable BC / MT / RT operation. To support the ACE the IP-1553 has an FPGA which provides the IP interface, clocking to the 1553 controller, interrupt processing, and other support functions.

The Micro-ACE part has many features including the following [taken from the DDC data sheet]

- # Fully Integrated 3.3 Volt, 1553 A/B Notice 2 Terminal
- # Transceiver Power-down Options
- # Enhanced Mini-ACE Architecture
- # Multiple Configurations: -- BC/RT/Monitor, 64K RAM
- # Supports 1553A/B Notice 2, McAir, STANAG 3838 Protocols
- # MIL-STD-1553, McAir, and MIL-STD-1760 Transceiver Options
- # Compatible With Mini-ACE and ACE Generations
- # Highly Autonomous BC with Built-In Message Sequence Controller
- # Choice of Single, Double, and Circular RT Buffering Options
- # Selective Message Monitor
- # Comprehensive Built-In Self-Test
- # Choice Of 10, 12, 16, or 20 MHz Clock Inputs

The internal decoding performed within the FPGA is synchronized to the 1553 clock. A frequency doubler is used to allow tighter timing control over the asynchronous interface that the ACE employs. With the tighter timing fewer wait-states are required for an access from the IP bus. The internal rate is 40 MHz and the ACE is provided a 20 MHz. reference.

The IP interface is 8 and 32 MHz compatible. When operating at 32 MHz the hardware interface is faster. The ACE provides a done signal which the local state-machine utilizes to determine the end of each transfer. Reads and Writes are performed with optimized interfaces. The ACE has registers and memory. Address 18 is used to select the ACE device and Address 17 to select between Register and Memory space within the ACE. The 64K memory within the ACE devices exceeds the size of the IP IO



space. The Memory space is used to decode the ACE addresses. The IO space is used to decode the control registers within the FPGA.

Each channel has a control register within the FPGA to set the channel specific options. Each channel has a portion of the IP Memory space allocated to allow direct offsets based on the ACE addresses to be utilized.

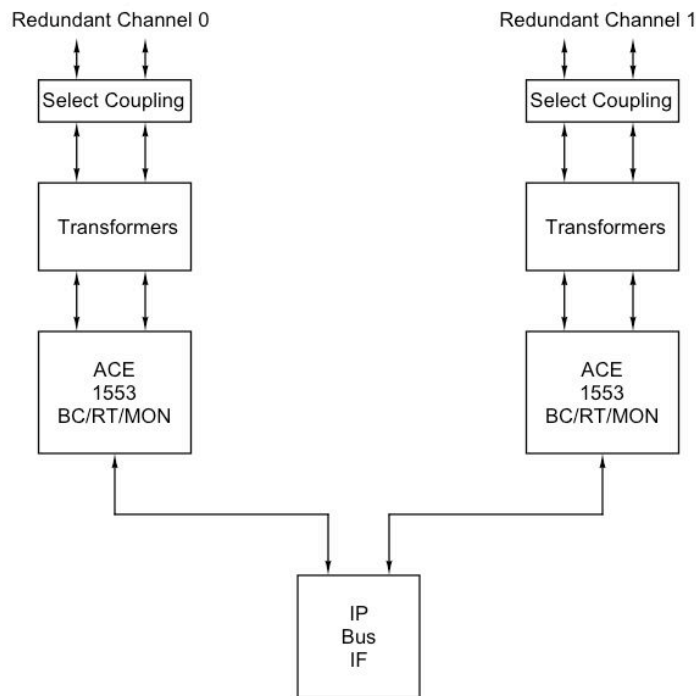


FIGURE 1 IP-1553 BLOCK DIAGRAM  
All FPGA configuration registers support read and write operations for maximum software convenience. The ACE has register dependent R/W capability.

IP-1553 conforms to the IndustryPack® standard. This guarantees compatibility with compliant carrier boards. Because the IP-1553 may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCI3IP – PCI carrier for IP Modules can be used for development in a conventional PC. Later the hardware and software can be ported to the target.  
[http://www.dyneng.com/pci\\_3\\_ip.html](http://www.dyneng.com/pci_3_ip.html)

With the Dynamic Engineering Windows driver collection for IP and carrier modules a Parent – Child architecture is employed. The IP portion of the driver is directly portable



between the various Dynamic Engineering IP carriers [PCI3IP, PCI5IP, PC104pIP, PC104p4IP, cPCI2IP, cPCI4IP etc]. The parent portion of the driver contains the carrier specific design information. This means that software developed for the IP-1553 on one platform can be directly ported to another. PCI to cPCI for example.

Designers can even make use of the Dynamic Engineering carrier driver for non Dynamic Engineering IP modules using the Generic IP capability built into the parent portion of the driver. IP modules that the carrier driver does not recognize are installed as “generic” and accessed with a address, data interface model. Software developed for the Generic mode can also be ported between modules.

IP-1553 is tested with a combination of internal and external tests. The registers can be tested with R/W tests, the channels can be tested with selftests, and the channels can be tested with an interchannel loop test. The ATP for IP-1553 includes FPGA internal, Local to ACE [RAM, Protocol, Register] and loop-back tests.

Interrupts are supported by IP-1553 The ACE has several programmable interrupts for RX, TX and error conditions. Each channel has a separate interrupts and enables. All interrupts are individually maskable. In addition a board level SW interrupt is provided for test and software development purposes.

IP-1553 is implemented with the idea of offloading the CPU as much as possible. The ACE has internal RAM to cut down on the number of interrupts to deal with. With address masking only the messages of interest can be received to further reduce CPU traffic. Most registers retain their information between messages allowing for quick reload and send once the initial programming has been implemented.

The ACE Transceivers are coupled to the MIL-STD-1553 bus via on-board transformers. The transformers have multiple taps to support direct and transformer coupled connections to the main bus. The Direct and Transformer coupled options are provided with shunts and the J2 /J3 header blocks. 54.9  $\Omega$  resistors are provided in the Direct coupled path.

The ACE devices can be programmed to use an external clock and support and external trigger. The signals are routed from the IO connector through the FPGA to the ACE devices. If further conditioning is required please contact Dynamic Engineering.

In addition the RTA address and parity bit are provided on the IO connector and terminated with pull-ups. The signals can be programmed with software or within the cable. Separate addresses are provided for each channel.



## Address Maps

### Address Map Internal

IP_1553_BASE	0x0000	// 0 base control register offset
IP_1553_VECTOR	0x0002	// 1 Vector Register offset
IP_1553_STATUS	0x0004	// 2 Base Status register
IP_1553_ControlReg0	0x0014	// 10 Channel 0 control register
IP_1553_StatusReg0	0x0016	// 11 Channel 0 status register
IP_1553_ControlReg1	0x0028	// 20 Channel 1 control register
IP_1553_StatusReg1	0x002A	// 21 Channel 1 status register

FIGURE 2

IP-1553 INTERNAL ADDRESS MAP



```
// IP-1553 relative addresses //
// ACE Controller internal accesses are on word boundaries in Memory Space
// Channel 0/1 is offset based on address 18
// Memory versus Register based on address 17
```

## Address Map Channel 0

```
#define IMR1_0      0x00000 //0 R/W
#define CR1_0      0x00002 //1 R/W
#define CR2_0      0x00004 //2 R/W
#define SRR_0      0x00006 //3 WR
#define CSP_0      0x00006 //3 RD
#define BC_COUNT_0 0x00008 //4 R/W
#define TIME_TAG_0 0x0000a //5 R/W
#define ISR1_0     0x0000c //6 RD
#define CR3_0      0x0000e //7 R/W
#define CR4_0      0x00010 //8 R/W
#define CR5_0      0x00012 //9 R/W
#define RT_MON_SAR_0 0x00014 //a RD
#define BC_FTR_0   0x00016 //b RD
#define BC_TRNM_0  0x00018 //c RD
#define AUX1_0     0x0001a //d RW Enhanced mode
#define FRAMETIME_0 0x0001a //d RW
#define RT_STAT_0  0x0001c //e RD only
#define RT_BIT_0   0x0001e //f RD only
#define TMR0_0     0x00020 //10
#define TMR1_0     0x00022 //11
#define TMR2_0     0x00024 //12
#define TMR3_0     0x00026 //13
#define TMR4_0     0x00028 //14
#define TMR5_0     0x0002a //15
#define TMR6_0     0x0002c //16
#define TMR7_0     0x0002e //17
#define CR6_0      0x00030 //18 R/W
#define CR7_0      0x00032 //19 R/W
// address 1a = RESERVED
#define BC_CCR_0   0x00036 //1b RD
#define BC_GPF_0   0x00036 //1b WR
#define BIT_0      0x00038 //1c RD
#define IMR2_0     0x0003a //1d R/W
#define ISR2_0     0x0003c //1e RD
#define QP_0       0x0003e //1f RW

#define SPA_0      0x20200 //memory stack pointer address offset 0
#define SPA_RX_0   0x20000 //memory RX data offset
#define SPA_TAG_0  0x20002 //memory tag offset
```

FIGURE 3 IP-1553 CHANNEL 0 ADDRESS MAP



## Address Map Channel 1

```
#define IMR1_1      0x40000 //0 R/W
#define CR1_1      0x40002 //1 R/W
#define CR2_1      0x40004 //2 R/W
#define SRR_1      0x40006 //3 WR
#define CSP_1      0x40006 //3 RD
#define BC_COUNT_1 0x40008 //4 R/W
#define TIME_TAG_1 0x4000a //5 R/W
#define ISR1_1     0x4000c //6 RD
#define CR3_1      0x4000e //7 R/W
#define CR4_1      0x40010 //8 R/W
#define CR5_1      0x40012 //9 R/W
#define RT_MON_SAR_1 0x40014 //a RD
#define BC_FTR_1   0x40016 //b RD
#define BC_TRNM_1  0x40018 //c RD
#define AUX1_1     0x4001a //d RW Enhanced mode
#define FRAMETIME_1 0x4001a //d RW
#define RT_STAT_1  0x4001c //e RD only
#define RT_BIT_1   0x4001e //f RD only
#define TMR0_1     0x40020 //10
#define TMR1_1     0x40022 //11
#define TMR2_1     0x40024 //12
#define TMR3_1     0x40026 //13
#define TMR4_1     0x40028 //14
#define TMR5_1     0x4002a //15
#define TMR6_1     0x4002c //16
#define TMR7_1     0x4002e //17
#define CR6_1      0x40030 //18 R/W
#define CR7_1      0x40032 //19 R/W
// address 1a = RESERVED
#define BC_CCR_1   0x40036 //1b RD
#define BC_GPF_1   0x40036 //1b WR
#define BIT_1      0x40038 //1c RD
#define IMR2_1     0x4003a //1d R/W
#define ISR2_1     0x4003c //1e RD
#define QP_1       0x4003e //1f RW

#define SPA_1      0x60200 //memory stack pointer address offset 0
#define SPA_RX_1   0x60000 //memory RX data offset
#define SPA_TAG_1  0x60002 //memory tag offset
```

FIGURE 4 IP-1553 CHANNEL 1 ADDRESS MAP



# Programming

Programming IP-1553 requires only the ability to read and write data from the host. The base address refers to the first user address for the slot in which the IP is installed.

Depending on the software environment it may be necessary to set-up the system software with IP-1553 "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware. Other OS may be more "plug and play". The Dynamic Engineering Driver operates in a "plug and play" mode with a parent ⇔ child architecture.

In order to receive and or transmit data the software is required to enable the controller for the channel(s) of interest. The initialization procedure is a mult-step process determined by the ACE BU64863, and the desired mode of operation. It is recommended that the user who is writing their own driver refer to the DDC Application notes for the BU64863.

Interrupts are used to help manage the data transfer process. When a programmed transfer is completed the interrupt can be generated to alert the host to program a new transfer. The transfers are independent for each channel allowing the CPU interaction to be minimized.

The Dynamic Engineering IP-1553 driver for Windows 2000 and XP manages the interaction and can set-up the transfer for you. The driver is easily integrated into a Visual C programming environment. Please refer to the driver manual for more information.



# Register Definitions

## IP\_1553\_BASE

IP\_1553\_BASE 0x0000 // 0 base control register offset

BASE Control Register	
DATA BIT	DESCRIPTION
15-1	Spare
0	INTFORCE

FIGURE 5

IP-1553 BASE CONTROL REGISTER BIT MAP

Intforce when set causes an interrupt to be generated to the system. Useful for debugging and software test.

## IP\_1553\_VECTOR

IP\_1553\_Vector                      0x0002 // 1 IP vector port

<b>Vector Port</b>	
<b>DATA BIT</b>	<b>DESCRIPTION</b>
15-8	Spare
7-0	vector

FIGURE 6

IP-1553 VECTOR BIT MAP

If the system uses a vectored interrupt approach then the vector port should be initialized to the vector value assigned to this device. IP-1553 is designed to be used as vectored or auto-vectored. In auto-vectored situations this port is unused. The Status port can be used to determine the source of any pending interrupts from IP-1553.

Default is 0xFF for data.



## IP\_1553\_STATUS

IP\_1553\_STATUS

0x0004 // 2 base Status register

CONTROL RX	
DATA BIT	DESCRIPTION
15-7	Spare
6	CH1_INT
5	Spare
4	CH0_INT
3-1	Spare
0	LOC_INT

FIGURE 7

IP-1553 INTERRUPT STATUS BIT MAP

LOC\_INT is set when INTFORCE, CHO\_INT or CH1\_INT are set and the corresponding mask is enabled. This bit is cleared by dealing with the interrupt source.

CH0\_INT and CH1\_INT are the interrupts from channel 0 and channel 1 1553 interface devices. The bits are before the interrupt mask and will be set even if the channel interrupt mask is not set to allow polled operation.

The interrupt signals are inverted in hardware to provide an active high status. Each interrupt can be enabled to be set from a variety of sources. Please refer to the IMR, registers for channel based interrupt control.



## IP\_1553\_ControlReg0, IP\_1553\_ControlReg1

IP\_1553\_ControlReg0,1                      0x0014,0x0028 // 10,20

CHANNEL CONTROL REGISTER	
DATA BIT	DESCRIPTION
15	Interrupt Mask
14	SLEEPN
13	RSTBITN
12	CH_RSTN
11-0	Spare

FIGURE 8

IP-1553 LOCAL CONTROL BIT MAP

CH\_RSTN is tied to the RSTN [MSTCLR] line on the ACE. When '0' the ACE is held in reset. When '1' the ACE can operate normally.

RSTBITN when set to '0' and the ACE brought out of reset will cause the ACE to do a BIT test. If this bit is set to '1' the BIT test is not performed. BIT can also be commanded through the SRR register. If using automatic BIT the ACE registers will not be writeable until the BIT completes. The BIT register can be used to determine when the test is complete or a timer set.

SLEEPN when '1' allows the ACE to go into a low power mode [transceivers]. Normally set to '0'.

Interrupt Mask when set '1' enables the channel interrupt to cause an IP level interrupt. When '0' the interrupt from the channel can still be used as a status bit, and the interrupt will not cause an IP level interrupt.



## IP\_1553\_StatusReg0, IP\_1553\_StatusReg1

IP\_1553\_StatusReg0,1                    0x0016,0x002A // 11,21

CHANNEL CONTROL REGISTER	
DATA BIT	DESCRIPTION
15-1	Spare
0	Channel Interrupt Status CHx_INT

FIGURE 9

IP-1553 LOCAL STATUS BIT MAP

Unmasked status bit for 1553 interrupt. Same status copied in board level status register. Clear by programming action with ACE device for appropriate channel.



## Interrupts

IP-1553 interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with an IP-1553 interrupt the software must read the status register(s) to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

The interrupt is mapped to INT0 on the IP connector, which is mapped to a system interrupt via the host [carrier] device. The source of the interrupt is obtained by reading the Interrupt Status register. The status remains valid until that bit in the status register is cleared.

When an interrupt occurs, the Master channel interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the status and enable the channel interrupt again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the Interrupt Status register.



## Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable with the following pins connected. Channel 0A to Channel 0B and channel 1A to channel 1B.

<u>SIGNALs</u>	<u>0</u>	<u>1</u>
CH0AP/CH0BP	27	33
CH0AN/CH0BN	29	35
CH1AP/CH1BP	43	48
CH1AN/CH1BN	45	50

In addition either 78 or 39 ohms between P & N is added for termination depending on shunt position.

## Select Direct/Transformer Coupled

J2 is used with Channel 0. J3 is used with channel 1. Each has 4 pieces to allow 4 shunts to be installed to select the P&N for A&B on each channel. 1-2 = Direct Coupled with 54.9Ω resistors in the path and requiring 39Ω termination. 2-3 = transformer coupled and uses the 78Ω termination resistor. We use two IP-Debug-IO cards with the two resistor values set plus loop-back wiring to make the loop-back test fixture. The IP-Debug-IO has two sets of connections allowing the wiring to be added in one set and the resistors in the alternate set.



## ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IP's I/O space, or at IP-base + \$80. Macintosh drivers use the ID PROM automatically.

Standard data in the ID PROM on the IP-1553 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification.

Address	Data
01	ASCII "I" (\$49)
03	ASCII "P" (\$50)
05	ASCII "A" (\$41)
07	ASCII "H" (\$48)
09	Manufacturer ID (\$1E)
0B	Model Number (\$0B) IP-1553
0D	Revision (\$B1)
0F	reserved (\$00) Customer Number
11	Driver ID, low byte (\$00) Design Number
13	Driver ID, high byte (\$00)
15	No of extra bytes used (\$0C)
17	CRC (\$E1)

FIGURE 10

IP-1553 ID PROM



## IP-1553 Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-1553. Pins marked n/c below are defined by the specification, but not used on the IP-1553. Also see the User Manual for your carrier board for more information.

GND		GND		1	26	
Reset*	CLK	R/W*	+5V	2	27	
D1	D0	n/c	IDSEL*	3	28	
D3	D2	n/c	MEMSEL*	4	29	
D5	D4	n/c	INTSEL*	5	30	
D7	D6	n/c	IOSEL*	6	31	
D9	D8	n/c	A1	7	32	
D11	D10	n/c	A2	8	33	
D13	D12	n/c	A3	9	34	
D15	D14	n/c	INTREG0*	10	35	
BS0*	BS0*	n/c	A4	11	36	
n/c	n/c	n/c	A5	12	37	
+5V	+5V	Ack*	A6	13	38	
GND	GND	n/c	n/c	14	39	
				15	40	
				16	41	
				17	42	
				18	43	
				19	44	
				20	45	
				21	46	
				22	47	
				23	48	
				24	49	
				25	50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 11

IP-1553 LOGIC INTERFACE



## IP-1553 IO Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-1553. Also see the User Manual for your carrier board for more information.

			1	26	
		CH0AP	2	27	
			3	28	
		CH0AN	4	29	
			5	30	
RTAD0P			6	31	
RTAD04			7	32	
RTAD03		CH0BP	8	33	
RTAD02			9	34	
RTAD01		CH0BN	10	35	
RTAD00			11	36	
EXT-TAG-CLK		GND	12	37	
XTRIG0	GND		13	38	
XTRIG1		GND	14	39	
INCMD0	GND		15	40	
INCMD1		GND	16	41	
RTAD1P			17	42	
RTAD14		CH1AP	18	43	
RTAD13			19	44	
RTAD12		CH1AN	20	45	
RTAD11			21	46	
RTAD10			22	47	
		CH1BP	23	48	
			24	49	
		CH1BN	25	50	

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

FIGURE 12

IP-1553 CONNECTOR PINOUT



# Applications Guide

## Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs should be connected with standard 1553 cabling or twisted pair wiring for best results.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

**Watch the system grounds.** All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

**Power all system power supplies from one switch.** Connecting external voltage to the IP-1553 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, use the isolated version.

**Keep cables short.** Flat cables, even with alternate ground lines, are not suitable for long distances. IP-1553 does not contain special input protection. The connector is pinned out for a standard Header cable to be used. The twisted pairs are defined to match up with the IP-1553 pin definitions. It is suggested that this standard cable be used for most of the cable run.

**Custom cables** can be manufactured with discrete wire header and direct connection to your mating equipment.

**Terminal Block.** We offer a high quality 50-screw terminal block that directly connects to the ribbon cable. The terminal block can mount on standard DIN rails. HDRterm50 [<http://www.dyneng.com/HDRterm50.html>]

**We provide the components. You provide the system.** Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the 1553 devices rated voltages.



## Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-1553 is constructed out of 0.062 inch thick high temp FR4 material.

Through hole and surface mounting of components are used. IC sockets use screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of  $.89 \text{ W}/^{\circ}\text{C}$  for uniform heat. This is based upon the temperature coefficient of the base FR4 material of  $0.31 \text{ W}/\text{m}\text{-}^{\circ}\text{C}$ , and taking into account the thickness and area of the IP. The coefficient means that if  $.89 \text{ Watts}$  are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

## Thermal Considerations

The IP-1553 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.



## Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

<http://www.dyneng.com/warranty.html>

## Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

## Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is \$100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

## For Service Contact:

Customer Service Department  
Dynamic Engineering  
150 DuBois St Suite 3  
Santa Cruz, CA 95060  
831-457-8891  
831-457-4793 fax  
[support@dyneng.com](mailto:support@dyneng.com)



## Specifications

Host Interface:	IP Module 8 and 32 MHz capable
1553 Interface:	1/2 Redundant Channels with full protocol support
Tx Data rates generated:	Programmable. 20 MHz reference to ACE
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers [except vector] to 0.
Access Modes:	IO, Memory, ID, INT spaces (see memory map)
Wait States:	minimized based on programmed clock rate
Interrupt:	Channel interrupt for each 1553 channel Software interrupt
Onboard Options:	Most Options are Software Programmable. Shunt options for direct and transformer coupled operation
Interface Options:	IP IO connector routed through IP Carrier. ARINC 1553 compatible cable with proper termination recommended
Dimensions:	Type 1 IP Module.
Construction:	High temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	.89 W/°C for uniform heat across IP
Power:	Typical <b>XX</b> mA @ 5V in Direct Coupled Mode running channel to channel test
Temperature Range	Industrial Temperature rated -40 + 85C. Conformal Coating option for condensing environments



## Order Information

IP-1553-1	IP Module with 1 redundant MIL-STD-1553 channel
IP-1553-2	IP Module with 2 redundant MIL-STD-1553 channels ACE [BU64863] per channel
Eng Kit–IP-1553	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender Technical Documentation, 1. IP-1553 Schematic 2. IP-1553 Reference test software Data sheet reprints are available from the manufacturer’s web site reference software.

**Note:** *The Engineering Kit is strongly recommended for first time IP-1553 purchases.*

## Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as “Corresponding Hardware Revision.” This information is not guaranteed to be current or complete manufacturing data, nor is it part of the product specification.

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