**DYNAMIC ENGINEERING**
435 Park Dr., Ben Lomond, Calif. 95005
831-336-8891 **Fax** 831-336-3840
http://www.dyneng.com
sales@dyneng.com
Est. 1988

**User Manual**

# IP-Crypto

IP Module
KYK-13 Transfer Mode Interface
Plus
Digital Parallel Interface
23 HV Outputs
21 HV Inputs

Revision A3
Corresponding Hardware: Revision 01
Firmware [PROM] revision D

# IP-Crypto

Digital Parallel Interface
IP Module

**Dynamic Engineering**
435 Park Drive
Ben Lomond, CA 95005
831-336-8891
831-336-3840 FAX
www.dyneng.com



The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.


Manual Revision A3. Revised 2/1/04

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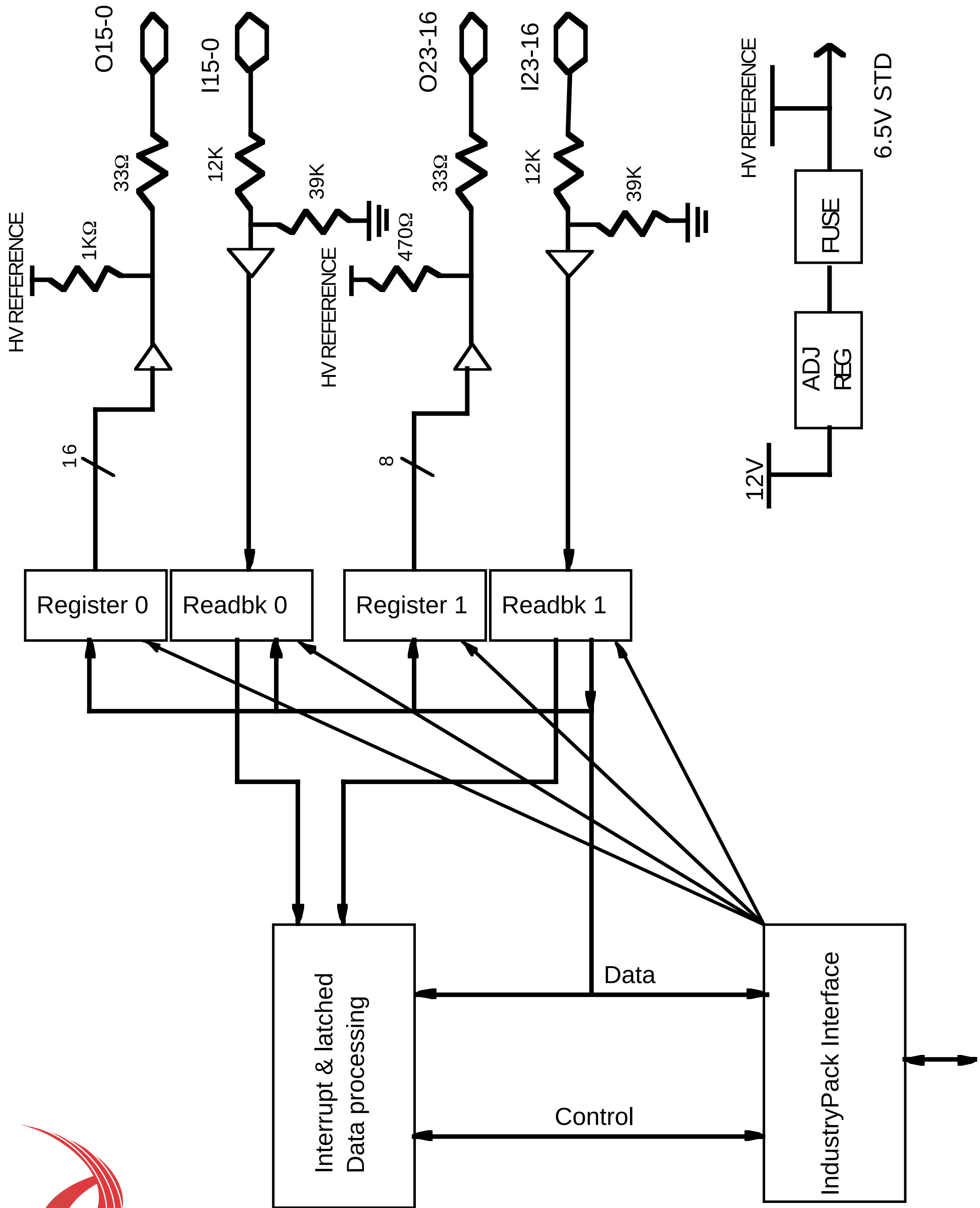
# Product Description and Operation



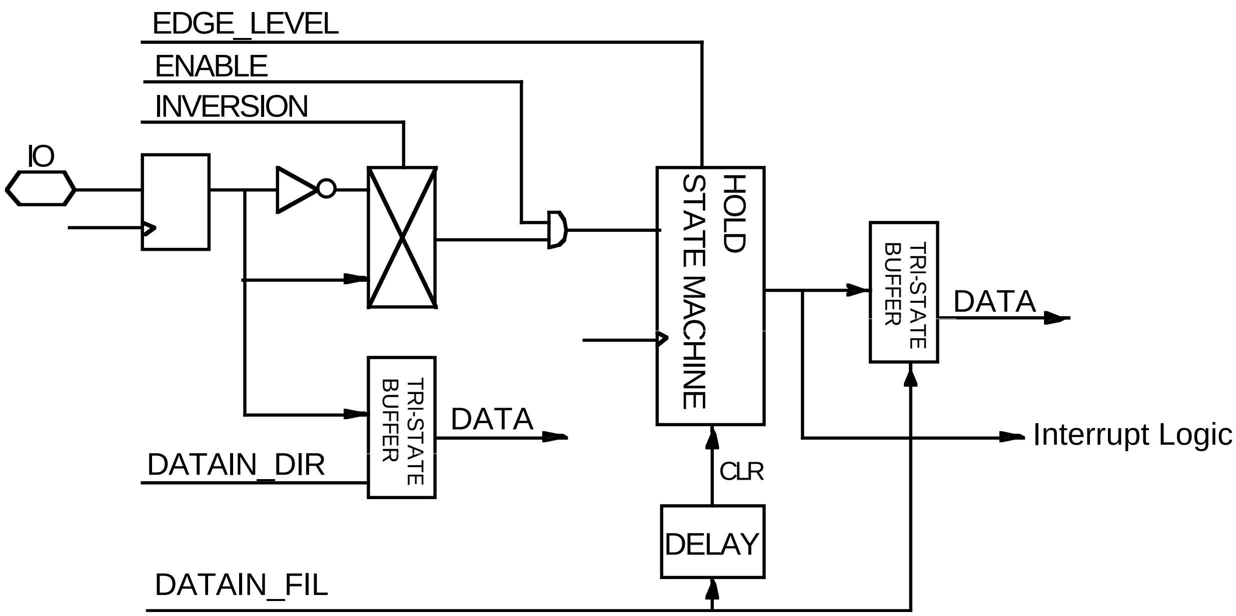
IP-Crypto is part of the IP Module family of modular I/O components. The IP-Crypto is a special version of the IP-Parallel-HV implementing a protocol compatible with the KYK-13 transfer mode interface. The standard version provides 24 uncommitted outputs and 24 uncommitted inputs. The IP-Crypto uses 1 output and 3 inputs for the Crypto interface. The outputs utilize LS07's to provide a high voltage low side switch. The on-board regulator provides a 6.5V standard reference. Other voltages can be supplied up to 12V. An external supply can be used when desired or if voltages above 12V need to be generated. Each input channel has a resistor divider to scale the input voltage back to "TTL" levels. The resistors can be altered for other voltage requirements.

Each output channel has a register bit associated with it. When the register bit is set to '0' that channel turns on the open-collector driver and puts a '0' on the line. When the register bit is set to '1' then the open collector driver is turned off and the pull-up will effect a high level on the line unless some other system element is driving the line low. The register is read-write and will always return the value written to it. There are 24 output lines. 2 registers are dedicated to the output [X23-0] bus. X0 is used for the Transfer Request signal leaving X23-1 for user outputs.

The output bus is additionally supported by a control bit in the base control register. If the bit is disabled, then enabled after the control bits of interest are set into the output bus registers; all 23 outputs will be updated on the same clock edge. If left enabled then the outputs will be updated one clock after the register is updated. If disabled then the output control is held from the last enabled control setting. The reset default is 'FFFFFF' to turn the drivers off.

Each Input line is also brought into the FPGA. The input lines are available as a direct read or after filtering. The Input bits are independent of the Output bits. All of the input bits are brought into the direct and filter data paths. The data input bits used for the KYK-13 interface are also sent to the state-machine for processing.

Each Input channel has an enable, sense, and edge or level bit associated with it. The enable will block or enable a particular channel from being received into the filtered logic. The sense will either keep the current version or invert the data received. The edge or level control will make the hold circuit wait for an edge from 0 > 1 or react to a level. The hold circuit captures data and holds it until read. The data is registered at the chip edge and then again after the enable and inversion circuitry. Each channel has a separate hold circuit. If a signal is detected to be high then the signal is held until the data is read. With the inversion capability each channel can be programmed to "be high" or to transition to a high condition when the channel has something of interest. The registers are referenced to the IP clock and operate at 8 or 32 MHz depending on the slot configuration. Each group of channels has a separate read clear signal. The channels can be read in any order and not loose data. The circuit will capture pulses down to 2 reference clocks wide. 60 nS or 250 nS with the standard IP reference clock.




The active high signals are combined to create an interrupt request based on the captured and held data. If the master interrupt enable is "enabled" then the interrupt is passed onto the system. The interrupt is cleared by reading the data or disabling the master enable. The user can program each channel to use the edge or level condition. The edge is particularly useful for long duration signal where repeated interrupts are not desired. The alternate approach is to flip the sense bit and create an interrupt when the signal has switched to the opposite polarity. Instruction order is important. Once the interrupt is detected the sense needs to be switched before the interrupt is re-enabled or a second interrupt is likely to be generated. It is recommended to read from the filtered data path after the processing parameters are changed to clear any interrupts that are created by the changing filter parameters.

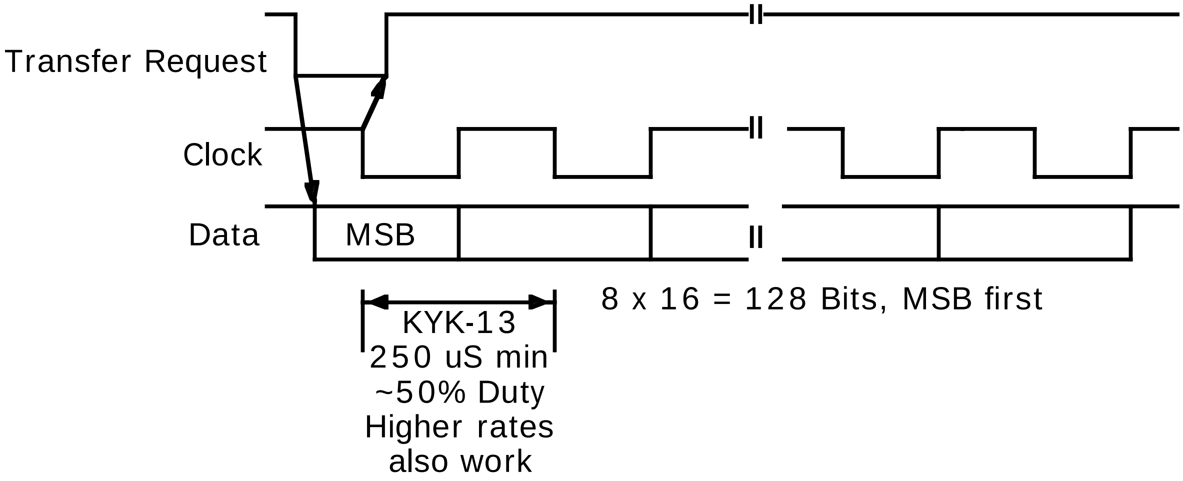
With each Input line having all three controls a lot of control possibilities exist. If desired the Inputs can be tied to the Outputs for loop-back and bi-directional control.

In addition to the IO version, other custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there, we will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a "standard" special order product. Please contact Dynamic Engineering with your custom application. Several of the Iinput bits are implemented on the long line clock pins of the FPGA. External clock references can be designed in as a custom option. There is a user oscillator position to support custom state machines and IO requirements. The DMA controls, second interrupt level, and memory space controls are routed to the FPGA to allow for future upgrades.

The IP-CRYPTO supports both 8 and 32 Mhz. IP Bus operation. All configuration registers support read and write operations for maximum software convenience. Word operations are supported (please refer to the memory map). The ID, IO, and INT spaces are utilized by the IP-Crypto design.

The IP-CRYPTO conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. The PCI3IP card makes a convenient development platform in many cases. http://www.dyneng.com/pci_3_ip.html

Interrupts are supported by the IP-CRYPTO. The interrupt occurs when a programmed transition occurs. The interrupts are individually maskable – each IO channel has a separate mask. The vector is user programmable by a read/write register. The interrupt occurs on IntReq0. The vector can be read in the IO space or automatically with the INT space.




The Transfer request signal is asserted when the software accesses the “trans” address with a write. Transfer Request remains asserted until the KYK-13 responds with the clock going low. Data changes on the rising edge and is captured by the IP-Crypto on the falling edge. The KYK-13 asserts data with inverted definitions. The IP-CRYPTO inverts the received data before the shift register to remove the inversion and to supply "normal" key information when read.

The KYK-13 interface specification defines the signal levels in terms of pin "A" on the KYK-13. The Crypto unit has a battery and internal logic. A '1' is a voltage = pin A +0 / -.1V. A '0' is Pin A voltage –5V [max] –6.5V [nominal] –6.8V Min. The standard IP-Crypto uses a regulator to create a 6.5V reference which is interconnected with Pin A on the KYK-13 unit to shift the "A" reference voltage to be 6.5V causing a '1' to be 6.5 volts and a '0' to be 0 volts. The KYK-13 circuitry floats within the KYK-13 chassis. Please refer to the pin definition tables for an interconnection specification to help connect the IP-Crypto to the KYK-13.

The state machine samples the clock and data inputs and when the state machine detects the clock to have changed state captures one data bit within the sixteen bit serial to parallel shift register. The serial data and clock are registered using the IP clock as a reference and then re-registered with the shift-register and state machine. The clock enable is used to gate the clock on the shift register and pick off one bit per transition. The data is captured within a few IP clocks of the falling edge of the KYK-13 clock. Much higher data rates are possible than the KYK-13 is rated for.

Once the data is received by the shift register it is loaded into a register file that stores 8 sixteen bit words. The register file is fed by 4 four sources. A mux selects the data path from the shift register or one of three clear pattern registers. [Clear_1..3]. After data is stored the state machine interrupts the host processor to read the data. A timer is started and if the data is not read within 5 seconds [8 MHz IP clock] then the data is automatically purged from the register file by writing the three patterns to each of the registers and then comparing that the clearing pattern was properly written. Status_1 ..3 reflect the proper or improper completion of the wiping pattern. A second interrupt can be used to "know" when the Clear Key operation has completed. If the data is read normally within the 5 second window then the Clear Key operation happens early. The eighth read triggers the Clear Key function independent of the timer function to allow the hardware to be ready for a new transfer request at an earlier time.

There is a separate address which the software can use to cause a Clear Key function to occur. The Clear Key function will be ignored if the state machine is not in the "idle" state i.e. the previous command completed.

The abort bit to the state machine and a timer should be used to provide a recovery path if the KYK-13 does not respond properly. If the transfer request is initiated and a software timer set to an appropriate and long time-out value, then if the SM Interrupt is not received within the time-out period the abort bit can be used to re-initialize the state-machine and break out of waiting for the KYK-13 device.

Once the SM Interrupt is received the first data is valid in the register file. Read the data then look to see if the next data is ready. The register file requires 10 IP clocks to update. The Status register busy bit can be polled or a software timer set to account for the delay before the next data is in the last "read" location.

# Address Map

| Function | | Offset | Width | Type |
|---|---|---|---|---|
| cntl0 | EQU | $00 | word | read / write |
| cntl1 | EQU | $02 | word | read / write |
| trans | EQU | $04 | word | write |
| Base_cntl | EQU | $06 | word | read / write |
| Int En0 | EQU | $08 | word | read / write |
| Int En1 | EQU | $0A | word | read / write |
| readkyk | EQU | $0C | word | read |
| vector | EQU | $0E | word | read / write |
| Int EdgLvl0 | EQU | $10 | word | read / write |
| Int EdgLvl1 | EQU | $12 | word | read / write |
| clrkey | EQU | $14 | word | write |
| | | | | |
| Int Pol0 | EQU | $18 | word | read / write |
| Int Pol1 | EQU | $1A | word | read / write |
| clear1 | EQU | $1C | word | read / write |
| status | EQU | $1E | word | read / clear |
| dat_in_fil0 | EQU | $20 | word | read |
| dat_in_fil1 | EQU | $22 | word | read |
| clear2 | EQU | $24 | word | read / write |
| clear3 | EQU | $26 | word | read / write |
| | | | | |
| dat_in_dir0 | EQU | $28 | word | read |
| dat_in_dir1 | EQU | $2A | word | read |
| dat_in_dir2 | EQU | $2C | word | unused |
| | | | | |
| Parallel_IDPROM | | | byte on word boundary | read |

FIGURE 1 IP-CRYPTO INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-CRYPTO. The addresses are all offsets from a base address. The carrier board that the IP is installed into provides the base address.

## Programming

Programming the IP-CRYPTO requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Carrier board.

In order to receive data the software is only required to read from the "Direct" port. Alternatively the filtered data path can be programmed with the enable, Level and edge and then the Filtered data used. If desired, the interrupt can be enabled and the interrupt vector written to the vector register.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example, $40 is a valid user vector for the Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the mask should be set. The Level and Edge conditions programmed then the enables set to receive data. The incoming data can be pulsed. The hardware will hold any pulse or level detected until the data is read by the software.

Data is written to the Control [cntl] registers. Any active low bits are used to enable the open drain drivers. The drivers have 40 mA sink capability and overcome the pull-up to create a '0' on the bus. A '1' in a bit position turns off the driver leaving the pull-up to set the level to a '1'. Other hardware in the system can also pull the signal line to '0'.

A 32 bit write/read with some CPUs will result in two 16 bit accesses to the hardware with automatic incrementing addresses. The 32 bit access is quite a bit faster than a software loop. The PCI3IP is an example of a carrier that supports 32 bit to 16 bit mapping automatically. The lower 32 bits of the output, "data in filtered", and "data in direct" are on long word boundaries to utilize this feature if available. [ http://www.dyneng.com/pci_3_ip.html ]

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

## Register Definitions

### CNTL0

$00 Parallel Control Register Port read / write

| CONTROL REGISTER 0 | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 15-0 | cntl 15-0 output data control bits |

FIGURE 2 IP-CRYPTO CONTROL REGISTER 0 BIT MAP

### CNTL1

$02 Parallel Control Register Port read / write

| CONTROL REGISTER 1 | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 15-8 | spare |
| 7-0 | cntl 23-16 output data control bits |

FIGURE 3 IP-CRYPTO CONTROL REGISTER 1 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF' off state for
2. In TTL mode each CNTL bit directly corresponds to an Output bit.

**Base_CNTL**

$06 BISERIAL Control Register Port read / write

| CONTROL REGISTER BASE | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 15-6 | spare |
| 5 | state machine abort |
| 4 | enable SM interrupt |
| 3 | enable CK interrupt |
| 2 | force interrupt 1 = force |
| 1 | master interrupt enable 1 = enabled |
| 0 | output register control 1 = enabled |

FIGURE 4 IP-CRYPTO BASE CONTROL REGISTER BIT MAP

1. Output Register Control is used to control when the Control registers values are placed onto the output registers. If synchronization is needed set to '0' until the registers are written and then enable ['1']. The output bits will then be driven to the new state at the same time. Referenced to the IP Clock. If the bit is left in the '0' state, then the new control register values will not be output and the data will stay in the previous state. If the bit is left in the '1' state then the control outputs will change when the registers are independently updated.

2. INT_EN is the master interrupt enable. Default is 0. If set to 1 then if one or more of the filtered input data conditions is met an interrupt will be generated on level 0.

3. Force Interrupt is used to create an interrupt for test and software development purposes. Set the bit to cause an interrupt and clear the bit to remove the interrupt. The IO bits can be used for the same purpose if the filter controls are properly set.

4. Enable CK interrupt when '1' enables the state machine to cause an interrupt at the completion of the Clear Key function.

5. Enable SM interrupt when '1' enables the state machine to cause an interrupt when the data transfer has completed. There is no hardware timer. If the 128 clocks required are not received the hardware will forever wait. It is a good idea to set a software timer to guard against non-completion. The Filtered inputs can easily be used to detect if the clock or data is changing to help diagnose this condition.

6. State Machine Abort when '1' will force the state-machine to return to the idle state. Useful if the state-machine is "hung" waiting for a non-responsive KYK-13

device. When asserting abort be sure to remove the abort signal again or the state-machine will not start up again. Set to ‘1’ and then to ‘0’ to abort. No software delay required.

## INTerrupt Enable

Int_en0 $08 Parallel Control Register Port read / write

| Interrupt Enable DATA BIT | DESCRIPTION |
|---|---|
| 15-0 | int_en 15-0<br>Interrupt Enable 1 = enabled, 0 = disabled |

FIGURE 5 IP-CRYPTO INTERRUPT ENABLE 0 BIT MAP

Int_en1 $0A Parallel Control Register Port read / write

| Interrupt Enable DATA BIT | DESCRIPTION |
|---|---|
| 15-8 | spare |
| 7-0 | int_en 23-16<br>Interrupt Enable 1 = enabled, 0 = disabled |

FIGURE 6 IP-CRYPTO INTERRUPT ENABLE 1 BIT MAP

The data bits correspond to the Input lines. In the filtered path if the control register bit is set to 1 then the corresponding Input line is enabled to be a potential interrupter and to be captured by the hold circuit. The enable is applied after the inversion control.

**INTerrupt Edge_Lvl**

Edg_Lvl 0 $10 Parallel Control Register Port read / write

| EDGE_LVL | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 15-0 | Edg_Lvl 15-0<br>1 = edge, 0 = level |

FIGURE 7 IP-CRYPTO INTERRUPT EDG_LVL 0 BIT MAP

Edg_Lvl 1 $12 Parallel Control Register Port read / write

| EDGE_LVL | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 15-8 | spare |
| 7-0 | Edg_Lvl 23-16<br>1 = edge, 0 = level |

FIGURE 8 IP-CRYPTO INTERRUPT EDG_LVL 1 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is captured only if there is a transition from ‘0’ to ‘1’. If set to ‘0’ then anytime the IO line is detected to be ‘1’ the hold circuit will be set. The hold circuit will retain the data until read by the corresponding data_in_fi(x) is accessed. The hold circuits are after the enable and inversion in the pipeline.

**INTerrupt Polarity**

Pol 0 $18 Parallel Control Register Port read / write

| DATA BIT | Polarity<br>DESCRIPTION |
|---|---|
| 15-0 | POL 15-0<br>1 = invert, 0 = not inverted |

FIGURE 9 IP-CRYPTO INTERRUPT POL 0 BIT MAP

Pol 1 $1A Parallel Control Register Port read / write

| DATA BIT | Polarity<br>DESCRIPTION |
|---|---|
| 15-8 | spare |
| 7-0 | POL 23-16<br>1 = invert, 0 = not inverted |

FIGURE 10 IP-CRYPTO INTERRUPT POL 1 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is inverted. If set to '0' then no inversion is applied.

## Data Input Filtered

Datain_fil0 $20 Parallel Control Register Port read / write

| Filtered Data | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 15-0 | DATAIN_FIL 15-0 |

FIGURE 11 IP-CRYPTO INTERRUPT DATAIN_FIL0 BIT MAP

Datain_fil1 $22 Parallel Control Register Port read / write

| Filtered Data | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 7-0 | DATAIN_FIL 23-16 |

FIGURE 12 IP-CRYPTO INTERRUPT DATAIN_FIL1 BIT MAP

The data bits correspond to the IO lines after the filters have been applied. The data remains latched until the register is read. Both registers are independent for reading and clearing purposes. Read [clear] the registers after any control change to insure that no false positives are reported.

The interrupt request(s) are formed by the "anding" of the Filtered Input Register Data and the corresponding Interrupt mask bits. To clear the interrupt; read the stored data. The data is self clearing from a read. If more than one bit is set the software will have to store that information for subsequent processing.

**Data Input Direct**

Datain_dir0 $28 Parallel Control Register Port read / write

| Direct Data | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 15-0 | DATAIN_DIR 15-0 |

FIGURE 13 IP-CRYPTO INTERRUPT DATAIN_DIR0 BIT MAP

Datain_dir1 $2A Parallel Control Register Port read / write

| Direct Data | |
|---|---|
| **DATA BIT** | **DESCRIPTION** |
| 7-0 | DATAIN_DIR 23-16 |

FIGURE 14 IP-CRYPTO INTERRUPT DATAIN_DIR1 BIT MAP

The data bits correspond to the IO lines without filters being applied. The data is a direct reflection of the current state of the IO lines. Meta-stable protection registers are in place but no hold registers.

## IP-Crypto Special Addresses

### Trans

When the Transfer Request address [0x04] is accessed with a write; a transfer request is initiated. The State-machine, when in the idle state, waits for a Clear Key or Transfer Request access. Transfer Request causes the Transfer Request signal to be asserted. The signal remains asserted until the KYK-13 responds with an active clock. 128 bits are captured to create 8 – 16 bit words. At the end of the capture an interrupt is create [SM interrupt] which can be polled or used as an interrupt. The state machine waits for either the data to be read or the timer to expire then runs the Clear Key sequence.

### Clrkey

When the Clear Key address is accessed [0x14] with a write, and the state machine is in the idle state, the Clear Key sequence is initiated. The data stored into the Clear Pattern registers are written to the register file and then checked against the stored pattern. There are 8 registers and three patterns. 24 writes plus overhead for checking the result are required to complete the clearing process. Any data stored into the shift register is cleared by enabling the shift register to capture new data and over-writing the data with the input data for an extended period. At the end of each pattern write, the data is checked against the expected value. If the register data matches the stored value then the Status bit is set. Status_1 …Status_3 correspond to Clear Pattern 1 …3. The status is captured and held for software in the status register.

### Readkyk

The register file data is read through this port [0x0C]. 8 reads are needed to completely recover the key. The state machine detects the end of the read and moves the data forward within the register file. With a tight loop and fast hardware it is possible to try to read the data before the data has been moved forward. The delay is short and in most cases will not be an issue. If the key appears to be miss-read add a delay between reads.

### Clear Pattern

clear_1, clear_2, clear_3. [0x1C,0x24,0x26] The Clear Pattern registers are used to store the three patterns used to clear out the register file after the key has been read. The registers are read-writeable and 16 bits wide. Clear_1 is used first. Clear_3 is used last. The register file will end up with the Clear_3 pattern until read again or a new capture performed.

## Status Register

The status register [0x1E]  read only

| Status<br>DATA BIT | DESCRIPTION |
|---|---|
| 7 | RDY / BSY |
| 6-5 | unused set to '0' |
| 4 | SM INT RQST |
| 3 | STATUS_3 |
| 2 | STATUS_2 |
| 1 | STATUS_1 |
| 0 | CK INT RQST |

FIGURE 15 IP-CRYPTO STATUS BIT MAP

The bits contained in the Status Register are captured and held.  When written to with the corresponding bit set the bits in the Status Register are cleared.  The bits are active high.  '1' = good STATUS and '1' = active interrupt.  If the interrupt enable is also set then an interrupt will be driven to the host.  If the enable is not set then the status can be used to poll.

The RDY / BSY signal is not latched.  The RDY / BSY signal is set by the state-machine during the register read sequence to indicate when data is ready to be read.  When set data is ready.  When '0' the data is being updated and should not be read.  This bit can be polled.  It takes 10 IP clocks to move the data to the next position through-out the register file.  An alternate approach is to use a software timer to accomplish the delay.  Many OS support a 10 mS timer "tick" which is more than sufficient to account for the needed delay.  The bit is only valid after the state-machine has set the SM INT RQST bit and before the Clear Key function has started.  The bit has alternate definitions when read outside of the defined time.

## BIS_VECTOR

$0E Parallel Interrupt Vector Port

The Interrupt vector for the IP-Crypto is stored in this byte wide register. This read / write register is initialized to 'xxFF' upon power-on reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered. The interrupt is automatically cleared when the CPU acknowledges the interrupt.

## Interrupts

All IP Module interrupts are vectored. The vector from the IP-CRYPTO comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-CRYPTO state machines generate an interrupt request when a programmed condition is detected on the IO lines. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector and clear the request when accessed by the CPU. The source of the interrupt is obtained by reading DATA_IN_FIL0-1 or the Status register depending on the source. The status remains valid until the registers are cleared.

The KYK-13 portion of the interface uses the Status Register instead of the Filtered Data Register to capture and hold interrupt status. Interrupts associated with the KYK-13 interface are cleared by writing to the Status register with the corresponding data bit set.

Some carrier boards pre-fetch data. If your carrier board pre-fetches the interrupt status, then the status may be cleared when the SW goes to look at it. If this is an issue then be careful with the order of reading the registers to prevent the pre-fetching function from affecting operation.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BASE_CNTL register. The individual enables for IO lines are controllable through INT_EN0-1. The enable operates before the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to read the holding register [DATAIN_FIL0-1], reset the board, or disable the interrupt. The Interrupt acknowledge cycle fetches the vector, but does not clear the interrupt request in this design.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled.

## ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision to be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-CRYPTO is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-Crypto board will be recorded with a new code in the DRIVER ID and reserved fields.

| Address | Data | HV |
|---|---|---|
| 01 | ASCII "I" | $49 |
| 03 | ASCII "P" | $50 |
| 05 | ASCII "A" | $41 |
| 07 | ASCII "H" | $48 |
| 09 | Manufacturer ID | $1E |
| 0B | Model Number | $04 |
| 0D | Revision | $A0 |
| 0F | reserved | $01 |
| 11 | Driver ID, low byte | $01 |
| 13 | Driver ID, high byte | $00 |
| 15 | No of extra bytes used | $0C |
| 17 | CRC | $C9 |

FIGURE 16 IP-CRYPTO ID PROM

# IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-CRYPTO. Pins marked n/c below are defined by the specification, but not used on the IP-CRYPTO. Also see the User Manual for your carrier board for more information.

| | | | |
|---|---|---|---|
| GND | GND | 1 | 26 |
| CLK | +5V | 2 | 27 |
| Reset* | R/W* | 3 | 28 |
| D0 | IDSEL* | 4 | 29 |
| D1 | DMAReq0* | 5 | 30 |
| D2 | MEMSEL* | 6 | 31 |
| D3 | DMAReq1* | 7 | 32 |
| D4 | IntSel* | 8 | 33 |
| D5 | DMAck* | 9 | 34 |
| D6 | IOSel* | 10 | 35 |
| D7 | n/c | 11 | 36 |
| D8 | A1 | 12 | 37 |
| D9 | DMAEnd* | 13 | 38 |
| D10 | A2 | 14 | 39 |
| D11 | n/c | 15 | 40 |
| D12 | A3 | 16 | 41 |
| D13 | IntReq0* | 17 | 42 |
| D14 | A4 | 18 | 43 |
| D15 | IntReq1* | 19 | 44 |
| BS0* | A5 | 20 | 45 |
| BS1* | n/c | 21 | 46 |
| n/c | A6 | 22 | 47 |
| n/c | Ack* | 23 | 48 |
| +5V | n/c | 24 | 49 |
| GND | GND | 25 | 50 |

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 17 IP-CRYPTO LOGIC INTERFACE

# IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-CRYPTO. Pins marked. Also see the User Manual for your carrier board for more information.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| O_0 | | I_0 | | 1 | | 26 | |
| | O_1 | | I_1 | | 2 | | 27 |
| O_2 | | I_2 | | 3 | | 28 | |
| | O_3 | | I_3 | | 4 | | 29 |
| O_4 | | I_4 | | 5 | | 30 | |
| | O_5 | | I_5 | | 6 | | 31 |
| O_6 | | I_6 | | 7 | | 32 | |
| | O_7 | | I_7 | | 8 | | 33 |
| O_8 | | I_8 | | 9 | | 34 | |
| | O_9 | | I_9 | | 10 | | 35 |
| O_10 | | I_10 | | 11 | | 36 | |
| | O_11 | | I_11 | | 12 | | 37 |
| O_12 | | I_12 | | 13 | | 38 | |
| | O_13 | | I_13 | | 14 | | 39 |
| O_14 | | I_14 | | 15 | | 40 | |
| | O_15 | | I_15 | | 16 | | 41 |
| O_16 | | I_16 | | 17 | | 42 | |
| | O_17 | | I_17 | | 18 | | 43 |
| O_18 | | I_18 | | 19 | | 44 | |
| | O_19 | | I_19 | | 20 | | 45 |
| O_20 | | IO_20 | | 21 | | 46 | |
| | O_21 | | I_21 | | 22 | | 47 |
| O_22 | | I_22 | | 23 | | 48 | |
| | O_23 | | I_23 | | 24 | | 49 |
| VIO | | GND | | 25 | | 50 | |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 18 IP-CRYPTO IO INTERFACE

"O" 23-0 Correspond to the output signals and map directly to CNTL0,1 definitions. "I" 23-0 Correspond to the input signals and map directly to the direct and filtered data paths.

O0 is used for Transfer Request pin C on KYK-13
I1 is used for Data In Pin D on KYK-13
I2 is used for Clock In Pin E on KYK-13
I3 or any other input can be used for Switch In Pin B on KYK-13
VIO is used to source 6.5V in this design. Pin A on KYK-13. The DIODE protection allows external voltages to be input on this pin. With changes to the regulator settings [resistors] the on board regulator can be "programmed" for other reference voltages [12 V max output].

# Applications Guide

## Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

**Watch the system grounds**. All electrically connected equipment should have a fail safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point. Safety and reliability can be achieved only by careful planning and practice.

**Power all system power supplies from one switch.** Connecting external voltage to the IP-CRYPTO when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. The open collector outputs and resistor coupled inputs provide some protection.

**Proper Handling.**
Keep the module properly packaged in the factory sealed anti-static bag until ready to assembly onto your carrier at an approved anti-static workstation. Use proper handling procedures while installing the modules onto the carrier and the carrier into the system. Care in the assembly process can help avoid random failures in the field due to static discharge and other damage.

**Terminal Block**. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails.
[ http://www.dyneng.com/HDRterm50.html ]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

**Carriers**
Many companies have IndustryPack® carriers which can be used in your system. Dynamic Engineering is an active IP Module developer. We are adding more carriers to our product line. Please see our website for the current selection. As of this revision we have PCI, cPCI, and PC/104+ carriers.

## Loop-back Connections

The ATP software we use to test the IP-Crypto includes a loop-back test. The Engineering Kit for the IP-Crypto includes the source code for the ATP. The loop-back test is facilitated with an IP-Debug-IO card with added wire-wrapped interconnections.

Model "HV"

| From | To | Signal |
|---|---|---|
| 49 | 24 | I23 – O23 |
| 48 | 23 | I22 – O22 |
| 47 | 22 | I21 – O21 |
| 46 | 21 | I20 – O20 |
| 45 | 20 | I19 – O19 |
| 44 | 19 | I18 – O18 |
| 43 | 18 | I17 – O17 |
| 42 | 17 | I16 – O16 |
| 41 | 16 | I15 – O15 |
| 40 | 15 | I14 – O14 |
| 39 | 14 | I13 – O13 |
| 38 | 13 | I12 – O12 |
| 37 | 12 | I11 – O11 |
| 36 | 11 | I10 – O10 |
| 35 | 10 | I9 – O9 |
| 34 | 9 | I8 – O8 |
| 33 | 8 | I7 - O7 |
| 32 | 7 | I6 - O6 |
| 31 | 6 | I5 - O5 |
| 30 | 5 | I4 - O4 |
| 29 | 4 | I3 - O3 |
| 28 | 3 | I2 - O2 |
| 27 | 2 | I1 - O1 |
| 26 | 1 | I0 - O0 |

## Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-CRYPTO is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required. *Please order standard mounting kit for IPs if you want this option*. [IP-MTG-KIT]

The IP Module provides a low temperature coefficient of 0.89 W/$^{o}$C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-$^{o}$C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

### Thermal Considerations

The IP-Crypto design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

## Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

## Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

### Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

## For Service Contact:

Customer Service Department
Dynamic Engineering

435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
e-mail support@dyneng.com

# Specifications

| | |
|---|---|
| Logic Interface: | IP Module Logic Interface |
| Parallel Interface: | 24 open collector outputs. 40 mA sink with 470Ω [upper 8] or 1KΩ [lower 16] pull-up to reference Voltage.<br>24 Inputs with resistor divider.<br>Standard reference voiltages 6.5V, 5.85V |
| Software Interface: | Control Registers, ID PROM, Vector Register, Status Ports |
| Initialization: | Hardware Reset forces all registers to 0. |
| Access Modes: | Word I/O Space (see memory map)<br>Word in ID Space<br>Vectored interrupt |
| Access Time: | back-to-back cycles in 500ns (8Mhz.) or 125 nS (32 Mhz.) |
| Wait States: | 1 to all spaces |
| Interrupt: | Multiple interrupt filtering options available on each IO line. Enabled, Active hi or low, edge or level. |
| DMA: | No Logic Interface DMA Support implemented at this time. |
| Onboard Options: | All Options are Software Programmable |
| Interface Options: | 50 pin flat cable<br>50 screw terminal block interface [HDRterm50]<br>User cable |
| Dimensions: | Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches |
| Construction: | FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed. |
| Temperature Coefficient: | 0.89 W / $^{o}$C for uniform heat across IP |
| Power: | Max. **TBD** mA @ 5 |
| MTBF | 1.855 M hours Bellcore 25c GB |

# Order Information

The IP-Crypto board is a special configuration of the IP-Parallel-HV.
http://www.dyneng.com/ip_parallel_hv.shtml

| | |
|---|---|
| **"IP-Crypto"** | IP Module with 48 HV IO<br>24 [23] open collector drivers with 470Ω [upper 8] or 1KΩ [lower 16] pull-up to reference voltage<br>24 [22] Inputs with resistor divider network<br>16 bit IP interface<br>KYK-13 Transfer Mode Interface |
| Tools for IP-CRYPTO | IP-Debug-Bus - IP Bus interface extender with testpoints, isolated power and quickswitch technology to allow hot swapping of IPs or power cycling without powering down the host. http://www.dyneng.com/ipdbgbus.html<br><br>IP-Debug-IO II - IndustryPack IO connector breakout with testpoints, ribbon cable headers, and locations for user circuits. http://www.dyneng.com/ipdbgio.html<br><br>HDRterm50 - Ribbon cable compatible 50 pin header to 50 screw terminal header. Comes with DIN rail mounting capability. http://www.dyneng.com/HDRterm50.html<br><br>PCI3IP - 1/2 length PCI card with 3 IP slots. http://www.dyneng.com/pci_3_ip.html<br><br>PCI5IP - PCI card with 5 IP slots. http://www.dyneng.com/pci5ip.html<br><br>cPCI2IP - 3U cPCI card with 2 IP slots. http://www.dyneng.com/cpci2ip.html<br><br>IP-MTG-KIT – 4 metric stainless screw and stand-off pairs to retain IP-Crypto against the carrier board. Flat head screws match IP Specification mounting requirements. http://www.dyneng.com/IPHardware.html |