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User Manual

IP-QuadUART-485-PLRA

**IP Module Party Line Receiver Interface
Master/Target
8-bit TTL Parallel port with COS**

Revision B

Corresponding Hardware: Revision B

10-2002-1702

IP-QuadUART-485-PLRA
Party Line Receiver, Master / Target
IP Interface Module

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Table of Contents

PRODUCT DESCRIPTION	6
THEORY OF OPERATION	7
Interrupts	8
Programming	8
Address Map	9
Register Definitions	10
PLRA_BASE	10
PLRA_VECTOR	12
PLRA_XIL_REV	12
PLRA_POL	12
PLRA_MASK	13
PLRA_EDGEVL	13
PLRA_BOTH	13
PLRA_DOUT	14
PLRA_DIR	14
PLRA_DIRECT	14
PLRA_FILTER/PLRA_COS_CLR	15
PLRA_TX_DAT_LO	15
PLRA_TX_DAT_HI	15
PLRA_RX_DAT_LO	16
PLRA_RX_DAT_HI/PLRA_STAT_CLR	16
PLRA_TX_MDAT	16
PLRA_RX_MDAT	17
INTERRUPT STATUS	17
ID PROM	18
LOOP-BACK	19
IP MODULE IO INTERFACE PIN ASSIGNMENT	21
APPLICATIONS GUIDE	22
Interfacing	22
Construction and Reliability	23

Thermal Considerations	24
WARRANTY AND REPAIR	24
Service Policy	25
Out of Warranty Repairs	25
For Service Contact:	25
SPECIFICATIONS	26
ORDER INFORMATION	27



List of Figures

FIGURE 1	IP-QUADUART-485-PLRA ADDRESS MAP	9
FIGURE 2	IP-QUADUART-485-PLRA BASE CONTROL REGISTER	10
FIGURE 3	IP-QUADUART-485-PLRA VECTOR REGISTER	12
FIGURE 4	IP-QUADUART-485-PLRA XILINX REVISION REGISTER	12
FIGURE 5	IP-QUADUART-485-PLRA TTL POLARITY REGISTER	12
FIGURE 6	IP-QUADUART-485-PLRA TTL MASK REGISTER	13
FIGURE 7	IP-QUADUART-485-PLRA TTL EDGE/LEVEL REGISTER	13
FIGURE 8	IP-QUADUART-485-PLRA TTL BOTH EDGES REGISTER	13
FIGURE 9	IP-QUADUART-485-PLRA TTL DATA REGISTER	14
FIGURE 10	IP-QUADUART-485-PLRA TTL DIRECTION REGISTER	14
FIGURE 11	IP-QUADUART-485-PLRA TTL READ DIRECT REGISTER	14
FIGURE 12	IP-QUADUART-485-PLRA TTL READ FILTERED REGISTER	15
FIGURE 13	IP-QUADUART-485-PLRA TRANSMIT DATA LOW REGISTER	15
FIGURE 14	IP-QUADUART-485-PLRA TRANSMIT DATA HIGH REGISTER	15
FIGURE 15	IP-QUADUART-485-PLRA RECEIVE DATA LOW REGISTER	16
FIGURE 16	IP-QUADUART-485-PLRA RECEIVE DATA HIGH REGISTER	16
FIGURE 17	IP-QUADUART-485-PLRA TX MONITOR DATA REGISTER	16
FIGURE 18	IP-QUADUART-485-PLRA RX MONITOR DATA REGISTER	17
FIGURE 19	IP-QUADUART-485-PLRA INTERRUPT STATUS REGISTER	17
FIGURE 20	IP-QUADUART-485-PLRA ID PROM	18
FIGURE 21	IP-QUADUART-485-PLRA LOGIC INTERFACE	20
FIGURE 22	IP-QUADUART-485-PLRA IO INTERFACE	21

Product Description

IP-QuadUART-485-PLRA is part of the IP family of modular I/O components from Dynamic Engineering. This module provides a flexible interface for asynchronous communication with special features that allow more efficient IP bus utilization both in and out of the board.

The PLR interface provides communication with a DR11-C interface that resides in a PDP-11 computer. The IP-QuadUART-485-PLRA can be integrated into a PC, using a PCI IP carrier such as the PCI3IP or PCI5IP. The IP-QuadUART-485-PLRA generates a 24-bit serial word out, and receives a 16-bit data word from a variety of custom units. The 8 TTL bidirectional signals are user programmable with COS (change-of-state) capability. Interrupt generation capability is also available. The clock, data, monitor, strobe and external interrupt lines are all RS-485 differential I/O signals.

The PLRA can function as a master or target or both. As a master, there are three modes of operation. The strobe and monitor signals can be programmed to be active or suppressed to provide transmit/receiver (both active), transmit only (monitor not active), or receive only (strobe not active). The PLRA design also implements a target to facilitate loop-back testing. The target will capture transmitted data at 2 MHz and provide data when monitor is active. The differential Receive direction signals are terminated with 100 Ω resistors. For transmit direction signals, termination should be provided at the transmit signal destination.

The IP-QuadUART-485-PLRA supports both 8 and 32 MHz IP Bus operation. The IP Clock and an on-board oscillator are used to provide the reference clock for operation. The PLRA design will run at 2 MHz regardless of the IP clock rate. The standard value for the oscillator in location OCS-2 is 24 MHz.

The IP-QuadUART-485-PLRA conforms to the VITA standard for IP modules. This guarantees compatibility with multiple IP Carrier boards. Since the IP maintains plug-in and software compatibility while mounted on different form factors, system prototyping may be done on one IP Carrier board, with final system implementation done on a different one. In standard configuration it is a Type 1 mechanical with no components on the back of the board and one slot wide.

Interrupts are supported by the IP-QuadUART-485-PLRA. An external interrupt line can be programmed to cause an interrupt in various levels/edges. An interrupt is also provided when enabled bits from "filtered" TTL data are received. Messages transferred use a different interrupt resource. There is an interrupt that is used to support test verification. Interrupt signals can be read from the module status register. If the master interrupt enable is not set, interrupt status is still available to operate in polled mode.



Theory of Operation

The IP-QuadUART-485-PLRA is designed to implement a PDP-11, DR11-C function with programmable serial protocols in a single IP module.

The IP-QuadUART-485-PLRA features a Xilinx FPGA. The FPGA contains the IP and DR11-C interfaces as well as configuration and status registers for defining the interface between them, and to the external serial connections. Only the transceivers, and terminations are external to the Xilinx device.

The IP-QuadUART-485-PLRA is a part of the IP family of modular I/O products. It meets the IP Module Vita Standard. In standard configuration it is a Type 1 mechanical one slot wide. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document as well as basic logic design.

A logic block within the Xilinx device contains the decoding and timing elements required for the host CPU to interface with the IP bus. The timing is referenced to the 8 or 32 MHz IP logic clock. The IP responds to the ID, INT, and IO selects. The DMA control lines are connected to the Xilinx for future revisions, but are not used at this time. The IP-QuadUART-485-PLRA will convert a parallel 24-bit word (user created) to a serial differential data bit stream. The differential serial data, along with a differential clock, is driven to the users receiver at a 2 MHz rate.

A Strobe is used to signal the termination of each 24-bit word transmission. When the strobe enable bit is set, the falling edge of the clock pulse for the last bit will generate a strobe pulse that remains active for one clock period.

The user can generate a Monitor signal to sample data from the receiver unit interfaced to the IP-QuadUART-485-PLRA. Setting the Monitor enable bit in the base control register, will initiate the Monitor signal one clock cycle after the Strobe signal has been inactivated. Monitor is held active for 18 clock cycles, while differential data and clock are driven back to, and received by the IP-QuadUART-485-PLRA.

The 8-bit TTL interface is bidirectional, and is configured by the user. The user can read the TTL I/O bits directly or filtered based on user preference. The TTL inputs feature change-of-state detection (COS).



Interrupts

All IP Module interrupts can be used as “vectored”. The vector from the IP-QuadUART-485-PLRA comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8-bit value. The default value is \$FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector. The IP-QuadUART-485-PLRA also supports auto-vectored interrupts.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BASE_CONTROL register. Once the interrupt request is set, the way to clear the request is to reset the board, service the request, or disable the interrupt.

If operating in a polled mode and making use of the interrupts for status, the master interrupt should be disabled and the individual interrupts of interest enabled. When the STATUS register shows an interrupt pending the appropriate action can take place to clear the interrupt request.

Power on initialization will provide a cleared interrupt request, interrupts disabled, and interrupt vector of \$FF.

Programming

Programming the IP-QuadUART-485-PLRA requires only the ability to read and write data in the host's I/O space. The beginning address of the IO space for the slot that the IP is installed in is referred to, in this document, as the IP module base address. The IP Carrier board that the module is installed in determines the base address.

The IP clock (32 or 8 MHz) provides timing for the 2 MHz output clock, 24-bit word transmitted, the 16-bit word received, the strobe and the monitor.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example \$40 is a valid user vector for the Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the appropriate interrupt enables set. When an interrupt is received, first read the STATUS register to determine the source.

After setting up the interrupts, and setting the IP clock reference, set the transmit (upper and lower) data word. When the start bit is set, data is transmitted. An interrupt is set when the transmission is complete. Data can be changed and sent. If the monitor is enabled, the Rx data is valid when the interrupt is set.



Address Map

Name	Function	Offset	Width	Type
PLRA_BASE	Base control	0x00	word	read/write
PLRA_VECTOR	Vector	0x02	word	read/write
PLRA_XIL_REV	Xilinx revision	0x04	word	read
PLRA_POL	TTL filter polarity	0x06	word	read/write
PLRA_MASK	TTL filter mask	0x08	word	read/write
PLRA_EDGEVLV	TTL filter edge/level	0x0A	word	read/write
PLRA_BOTH	TTL filter both edges	0x0C	word	read/write
PLRA_DOUT	TTL output data value	0x0E	word	read/write
PLRA_DIR	TTL direction control	0x10	word	read/write
PLRA_DIRECT	TTL read direct data	0x12	word	read
PLRA_FILTER	TTL read filtered data	0x14	word	read
PLRA_COS_CLR	Clear COS interrupt	0x14	word	write
PLRA_TX_DAT_LO	Tx data 15-0	0x18	word	read/write
PLRA_TX_DAT_HI	Tx data 23-16	0x1a	word	read/write
PLRA_RX_DAT_LO	Rx data 15-0	0x1c	word	read
PLRA_RX_DAT_HI	Rx data 23-16, Status read	0x1e	word	read
PLRA_STAT_CLR	Status clear	0x1e	word	write
PLRA_TX_MDAT	Monitor data storage	0x20	word	read/write
PLRA_RX_MDAT	Receive data (Monitor req)	0x22	word	read
PLRA_INTSTAT	I/O Int Stat Read/Clear	0x24	word	read/write

FIGURE 1

IP-QUADUART-485-PLRA ADDRESS MAP

The address map provided is for the local decoding performed within the IP-QuadUART-485-PLRA. The addresses are all offsets from the IO space base address. The IDPROM is mapped to the ID space. The carrier board that the IP is installed into provides these addresses.

Register Definitions

PLRA_BASE

0x00 IP-QuadUART-485-PLRA Base Control Register [read/write]

BASE CONTROL REGISTER	
DATA BIT	DESCRIPTION
15	Start Bit for Master State-Machine
14	Start for Target State-Machine
13	Strobe Enable to Complete Write Output
12	Enable Monitor and Drive Read Clock
11	External Interrupt Enable
10	External Interrupt Both Edges
9	External Interrupt Edge/Level
8	External Interrupt Polarity
7	External Interrupt Mask
6	Stop Master State-Machine
5	Target Interrupt Out
4	IO Interrupt Enable
3	COS Interrupt Enable
2	Force Interrupt
1	Master Interrupt Enable
0	32 MHz Clock selected

FIGURE 2

IP-QUADUART-485-PLRA BASE CONTROL REGISTER

32 MHz Clock selected: set to '1' when 32 MHz IP clock is selected so that the state-machine timing will be consistent when the IP clock frequency changes. Set to a '0' when the 8 MHz IP clock is selected.

Master Interrupt Enable: when '1', enables interrupts onto the IP bus intreq0n line if any enabled interrupt conditions exist. When '0' (default state) no IP interrupt will occur regardless of any existing interrupt conditions.

Force Interrupt: is used to create an interrupt for test and software development purposes. Set the bit to cause the interrupt and clear the bit (default state) to remove the interrupt. It requires the master interrupt enable to be '1' to have an effect.

COS Interrupt Enable: generate an interrupt on the IP bus if a bit in the filtered latch is true. It requires the master interrupt enable to be '1' to have an effect.

IO Interrupt Enable: generate an interrupt on the IP bus when data transfer is complete. It requires the master interrupt enable to be '1' to have an effect.

Target Interrupt Out: generate an interrupt on the IP bus if the external interrupt input matches the change-of-state selected in the base control register. It requires the master interrupt enable to be '1' to have an effect.

Stop Master State-Machine: set to '1' to stop the master state-machine before it completes. Also requires start (bit 15) to be low during write. If neither start nor stop is a '1', the state-machine condition remains unchanged. This allows other bits to be altered in the base control register without interfering with the automatic clearing of the start bit.

External Interrupt Mask: when '1', enables external interrupt change-of-state detection. When '0' the external interrupt change-of-state circuit is disabled.

External Interrupt Polarity: when '1', inverts the polarity of the input to the external interrupt change-of-state detection circuit.

External Interrupt Edge/Level: when '1', the external interrupt change-of-state detection circuit only responds to a rising (polarity = '0') or falling edge (polarity = '1'). When '0' the change-of-state circuit responds to a high (polarity = '0') or low (polarity = '1') level.

External Interrupt Both Edges: when '1' and edge/level bit is also a '1', the external interrupt change-of-state circuit will respond to either a rising or falling edge.

External Interrupt Enable: when '1', enables the external interrupt to generate an interrupt on the IP bus when the programmed change-of-state occurs. It requires the master interrupt enable to be '1' to have an effect

Enable Monitor and Drive Read Clock: when set, generates a monitor signal that is held for minimum 18 clock cycles to enable a 16-bit serial word to be read back to the IP-QUADUART-485-PLRA.

Strobe Enable to Complete Write Output: when set, will generate a one period wide strobe signal whose rising edge occurs when the falling edge of clock of the last bit in a 24-bit serial write cycle.

Start for Target State-Machine: when set to '1', enables capture of 24-bit serial stream in target mode and if monitor is received to transmit 16-bit data.

Start for Master State-Machine: when set to '1', initiates a data transfer (See Strobe and Monitor control bits). This bit is cleared automatically when the master state-machine completes.

PLRA_VECTOR

0x02 IP-QuadUART-485-PLRA Interrupt Vector Register [read/write]

VECTOR REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	Interrupt Vector

FIGURE 3

IP-QUADUART-485-PLRA VECTOR REGISTER

The interrupt vector for the IP-QuadUART-484-PLRA is stored in this byte-wide register. This read/write register is initialized to 0XFF upon power-on reset or software reset. The vector is stored in the odd byte location [D7..0] and is driven onto the data bus during an interrupt acknowledge cycle. The vector should be initialized before the interrupt is enabled or the mask is lowered.

PLRA_XIL_REV

0x04 IP-QuadUART-485-PLRA Xilinx Revision Register [read only]

XILINX REVISION REGISTER	
DATA BIT	DESCRIPTION
15-0	Xilinx design revision number

FIGURE 4

IP-QUADUART-485-PLRA XILINX REVISION REGISTER

Xilinx design revision number: The value of register is the rev. number of the Xilinx design (currently 0x0002 - rev. B).

PLRA_POL

0x06 IP-QuadUART-485-PLRA TTL Polarity Register [read/write]

TTL POLARITY REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Change-of-State Filter Polarity

FIGURE 5

IP-QUADUART-485-PLRA TTL POLARITY REGISTER

TTL Change-of-State Filter Polarity: when '1' the corresponding TTL input bit change-of-state filter is inverted and will therefore capture a falling edge or low level depending on the state of the edge/level control bit. When '0', the filter is non-inverting and will capture a rising edge or high level.

PLRA_MASK

0x08 IP-QuadUART-485-PLRA TTL Mask Register [read/write]

TTL MASK REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Change-of-State Filter Mask

FIGURE 6

IP-QUADUART-485-PLRA TTL MASK REGISTER

TTL Change-of-State Filter Mask: when '1' the corresponding TTL input bit change-of-state filter is enabled to respond to the programmed state. When '0', the filter is disabled for that bit.

PLRA_EDGELVL

0x0A IP-QuadUART-485-PLRA TTL Edge/Level Register [read/write]

TTL EDGE/LEVEL REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Change-of-State Filter Edge/Level

FIGURE 7

IP-QUADUART-485-PLRA TTL EDGE/LEVEL REGISTER

TTL Change-of-State Filter Edge/Level: when '1' the corresponding TTL input bit change-of-state filter will respond to a rising or falling edge depending on the state of the polarity bit. When '0', the filter will respond to a logic level.

PLRA_BOTH

0x0C IP-QuadUART-485-PLRA TTL Both Edges Register [read/write]

TTL BOTH EDGES REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Change-of-State Filter Both Edges

FIGURE 8

IP-QUADUART-485-PLRA TTL BOTH EDGES REGISTER

TTL Change-of-State Filter Both Edges: when '1' the corresponding TTL input bit change-of-state filter will respond to either a rising or falling edge provided the edge/level bit is set. When '0', the filter will respond to only one edge.

PLRA_DOUT

0x0E IP-QuadUART-485-PLRA TTL Output Data Register [read/write]

TTL OUTPUT DATA REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Output Data Value

FIGURE 9

IP-QUADUART-485-PLRA TTL DATA REGISTER

TTL Output Data Value: sets the value of the corresponding TTL line when it is configured as an output (controlled by the PLRA_DIR register).

PLRA_DIR

0x10 IP-QuadUART-485-PLRA TTL Direction Register [read/write]

TTL DIRECTION REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Direction

FIGURE 10

IP-QUADUART-485-PLRA TTL DIRECTION REGISTER

TTL Direction: when '1' the corresponding TTL line will be configured as an output. When '0', the corresponding TTL line will be configured as an output.

PLRA_DIRECT

0x12 IP-QuadUART-485-PLRA TTL Read Direct Data Register [read only]

TTL READ DIRECT REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Read Direct Data

FIGURE 11

IP-QUADUART-485-PLRA TTL READ DIRECT REGISTER

TTL Read Direct Data: the raw value of the TTL lines can be read from this address.

PLRA_FILTER/PLRA_COS_CLR

0x14 IP-QuadUART-485-PLRA TTL Data Filter Register [read/write]

TTL COS FILTER REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	TTL Read/Clear Filtered Data

FIGURE 12

IP-QUADUART-485-PLRA TTL READ FILTERED REGISTER

TTL Read/Clear Filtered Data: the value of the TTL change-of-state latch is read from this register. If a TTL input bit has satisfied the programmed change-of-state settings since the latch was last cleared, it will be read as a one. Otherwise, it will be read as a zero. Writing a one to a bit in this register will clear the corresponding bit latch.

PLRA_TX_DAT_LO

0x18 IP-QuadUART-485-PLRA Transmit Data Low Word Register [read/write]

TRANSMIT DATA REGISTER	
DATA BIT	DESCRIPTION
15-0	Transmit Data Low

FIGURE 13

IP-QUADUART-485-PLRA TRANSMIT DATA LOW REGISTER

PLRA_TX_DAT_HI

0x1A IP-QuadUART-485-PLRA Transmit Data High Byte Register [read/write]

TRANSMIT DATA REGISTER	
DATA BIT	DESCRIPTION
15-8	Unused
7-0	Transmit Data High

FIGURE 14

IP-QUADUART-485-PLRA TRANSMIT DATA HIGH REGISTER

Transmit Data: these two registers are where the 24-bit transmit data is specified. This data is sent by the PLRA state-machine when it receives a start command.

PLRA_RX_DAT_LO

0x1C IP-QuadUART-485-PLRA Received Data Low Word Register [read only]

RECEIVE DATA REGISTER	
DATA BIT	DESCRIPTION
15-0	Receive Data Low

FIGURE 15

IP-QUADUART-485-PLRA RECEIVE DATA LOW REGISTER

PLRA_RX_DAT_HI/PLRA_STAT_CLR

0x1E IP-QuadUART-485-PLRA Received Data High Byte Register [read/write]

RECEIVE DATA REGISTER	
DATA BIT	DESCRIPTION
15	24-Bit Data Captured
14	Target Monitor Input
13-8	Spare
7-0	Receive Data High

FIGURE 16

IP-QUADUART-485-PLRA RECEIVE DATA HIGH REGISTER

Receive Data: these two registers report the 24-bit received data. This data has been received by the PLRA target state-machine.

Target Monitor Input: this bit reports the real-time state of the target monitor input to the board. This signal causes the target state-machine to output a 16-bit data response.

24-Bit Data Captured: this bit is latched by the target state-machine to indicate that it received a 24-bit command word. Writing back a one to this bit will clear the latch.

PLRA_TX_MDAT

0x20 IP-QuadUART-485-PLRA Transmit Monitor Data Register [read/write]

TRANSMIT MONITOR DATA REGISTER	
DATA BIT	DESCRIPTION
15-0	Transmit Monitor Data

FIGURE 17

IP-QUADUART-485-PLRA TX MONITOR DATA REGISTER

Transmit Monitor Data: this register is where the 16-bit monitor response data is specified. This data is sent by the target state-machine when it receives the monitor signal.

PLRA_RX_MDAT

0x22 IP-QuadUART-485-PLRA Received Monitor Data Register [read only]

RECEIVE MONITOR DATA REGISTER	
DATA BIT	DESCRIPTION
15-0	Receive Monitor Data

FIGURE 18

IP-QUADUART-485-PLRA RX MONITOR DATA REGISTER

Receive Monitor Data: this register reports the 16-bit monitor data received by the PLRA state-machine when the monitor signal is asserted.

INTERRUPT STATUS

0x24 IP-QuadUART-485-PLRA Interrupt Status Port [read/write]

INTERRUPT STATUS REGISTER	
DATA BIT	DESCRIPTION
15-3	Spare
2	External Interrupt Active
1	Change of State Interrupt Active
0	Data Transfer Complete

FIGURE 19

IP-QUADUART-485-PLRA INTERRUPT STATUS REGISTER

Data Transfer Complete: when '1' indicates that a data transfer has completed. This is cleared on reset or by writing back a one to bit 0 of this register.

Change of State Interrupt Active: when '1' indicates a change of state has occurred from one or more of the bits in the filtered data latch. If MASTER INT ENABLE is '1', IP Bus interrupt 0 will be asserted, otherwise this status bit allows polling of the interrupt condition. The interrupt is cleared on reset or by clearing the 8 bits of the COS latch.

External Interrupt Active: when '1' indicates a programmed change-of-state has occurred in the external interrupt input. If MASTER INT ENABLE is '1', IP Bus interrupt 0 will be asserted, otherwise this status bit allows polling of the interrupt condition. The interrupt is cleared on reset or by writing back a one to bit 2 of this register.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IP's I/O space, or at IP-base + \$80. Macintosh drivers use the ID PROM automatically.

Standard data in the ID PROM on the IP-QuadUART-485-PLRA is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Any modifications to the IP-QuadUART-485-PLRA board will be recorded with a new code in the DRIVER ID location. The model number is set to 0x07 with a customer number of 0x0A.

Address	Data	
01	ASCII "I"	(0x49)
03	ASCII "P"	(0x50)
05	ASCII "A"	(0x41)
07	ASCII "H"	(0x48)
09	Manufacturer ID	(0x1E)
0B	Model Number	(0x07)
0D	Revision	(0xB0)
0F	Customer	(0x0A)
11	Driver ID, low byte	(0x03)
13	Driver ID, high byte	(0x00)
15	No of extra bytes used	(0x0C)
17	CRC	(0x58)

FIGURE 20

IP-QUADUART-485-PLRA ID PROM

Loop-back

The Engineering kit has reference software, which includes an external loop-back test for each interface specification. Each test requires an external cable with the following pins connected.

RS-485 Loop-back

<u>Signal A</u>	<u>Signal B</u>	<u>From</u>	<u>To</u>
M_RX_CLKIN_X16 +	T_CLKOUT_X16 +	1	27
M_RX_CLKIN_X16 -	T_CLKOUT_X16 -	2	28
M_TX_CLKOUT_X24 +	T_CLKIN_X24 +	3	25
M_TX_CLKOUT_X24 -	T_CLKIN_X24 -	4	26
T_MONITOR +	M_MONITOR +	5	7
T_MONITOR -	M_MONITOR -	6	8
T_STROBE +	M_STROBE +	9	11
T_STROBE -	M_STROBE -	10	12
M_DATAIN_X16+	T_DATAOUT_X16+	13	39
M_DATAIN_X16-	T_DATAOUT_X16-	14	40
M_DATAOUT_X24+	T_DATAIN_X24+	15	37
M_DATAOUT_X24 -	T_DATAIN_X24-	16	38
TTL(0)	TTL(4)	17	41
TTL(1)	TTL(5)	19	43
M_INTERRUPT +	T_INTERRUPT +	29	31
M_INTERRUPT -	T_INTERRUPT -	30	32
TTL(2)	TTL(6)	33	45
TTL(3)	TTL(7)	35	47

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-QuadUART-485-PLRA. Pins marked n/c below are defined by the specification, but not used on the IP-QuadUART-485-PLRA. Also see the User Manual for your carrier board for more information.

GND		GND		1	26	
Reset*	CLK	R/W*	+5V	2	27	
D1	D0	n/c	IDSEL*	3	28	
D3	D2	n/c	MEMSEL*	4	29	
D5	D4	n/c	INTSEL*	5	30	
D7	D6	n/c	IOSEL*	6	31	
D9	D8	n/c	A1	7	32	
D11	D10	n/c	A2	8	33	
D13	D12	n/c	A3	9	34	
D15	D14	n/c	INTREQ0*	10	35	
BS1*	BS0*	n/c	A4	11	36	
+12V	-12V	n/c	A5	12	37	
GND	+5V	Ack*	A6	13	38	
		GND	n/c	14	39	
				15	40	
				16	41	
				17	42	
				18	43	
				19	44	
				20	45	
				21	46	
				22	47	
				23	48	
				24	49	
				25	50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 21

IP-QUADUART-485-PLRA LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-QuadUART-485-PLRA. Also see the User Manual for your carrier board for more information.

M_RX_CLKIN_X16+	T_CLKIN_X24-	1	26
M_RX_CLKIN_X16-	T_CLKOUT_X16+	2	27
M_CLKOUT_X24+	T_CLKOUT_X16-	3	28
M_CLKOUT_X24-	M_INTERRUPT+	4	29
T_MONITOR+	M_INTERRUPT-	5	30
T_MONITOR-	T_INTERRUPT+	6	31
M_MONITOR+	T_INTERRUPT-	7	32
M_MONITOR-	TTL(2)	8	33
T_STROBE+	NOT USED	9	34
T_STROBE-	TTL(3)	10	35
M_STROBE+	NOT USED	11	36
M_STROBE-	T_DATAIN_X24+	12	37
M_DATAIN_X16+	T_DATAIN_X24-	13	38
M_DATAIN_X16-	T_DATAOUT_X16+	14	39
M_DATAOUT_X24+	T_DATAOUT_X16-	15	40
M_DATAOUT_X24-	TTL(4)	16	41
TTL(0)	NOT USED	17	42
NOT USED	TTL(5)	18	43
TTL(1)	NOT USED	19	44
NOT USED	TTL(6)	20	45
NOT USED	NOT USED	21	46
NOT USED	TTL(7)	22	47
NOT USED	NOT USED	23	48
NOT USED	GND*	24	49
T_CLK_IN_X24+	GND*	25	50

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 22

IP-QUADUART-485-PLRA IO INTERFACE

The pin definition for the IP-QuadUART-485-PLRA was chosen for compatibility with existing products to minimize the cost of migration.

GND* The grounds are tied to the local ground plane via 0Ω resistor. Optionally a capacitor or open can be installed to create DC, AC, or isolated references depending on your interfacing needs. DC coupled is the default. –AC will install a .1 uF cap. –OPN will leave the position open. Please note that the GNDs will still be tied together just unreferenced on the IP-QuadUART-485-PLRA.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. RS-485 components are designed to handle the mis-matched power references experienced in distributed networks. It is always a good idea to try to minimize the differences in power references and on-off states. If you will have large differences in power which might exceed the maximum of the RS-485 transceivers please contact the factory.

Terminal Block. We offer a high quality 50-screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails.

[\[http://www.dyneng.com/HDRterm50.html\]](http://www.dyneng.com/HDRterm50.html)

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

IndustryPack® Carriers Dynamic Engineering offers IP module carriers for PCI, PC104P, and cPCI implementations. Third party companies offer carriers for VME.

<http://www.dyneng.com/pci5ip.html> is the URL for a 5 slot, PCI carrier.

http://www.dyneng.com/pci_3_ip.html is the URL for a 3 slot, PCI carrier.

<http://www.dyneng.com/cpci4ip.html> is the URL for a 4 slot, cPCI 6U carrier.

<http://www.dyneng.com/cpci2ip.html> is the URL for a 2 slot, cPCI 3U carrier.

<http://www.dyneng.com/pc104p4ip.html> is the URL for a 4 slot, PC104P carrier.

http://www.dyneng.com/pc104p_ip.html is the URL for a 1 slot PC104P carrier.

Debugging – IP Modules are supported with integration aides and engineering kits. The IP-Debug-IO and IP-Debug-Bus provide isolation and testpoints on the IO and Logic connectors for an IP Module. The IP-Debug-Bus provides power isolation, testpoints, and a reset switch to allow hot-swapping of IP hardware while in test. The IP-Debug-IO attaches to the IO connector and provides a connection to standard ribbon cable and testpoints for your measurement equipment. The IP-Debug-IO has positions for adding components in case you need to simulate part of your system.

<http://www.dyneng.com/ipdbgio.html> is the URL for the IP-Debug-IO.

<http://www.dyneng.com/ipdbgbus.html> is the URL for the IP-Debug-Bus.



Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-QuadUART-485-PLRA is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of 0.89 W/°C for uniform heat dissipation. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-QuadUart-485-PLRA design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air-cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.



Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is \$100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 Fax
Internet Address support@dyneng.com



Specifications

Logic Interface:	IP Module Logic Interface
Serial Interface:	RS-485: Clk, Data, Monitor, Strobe, Interrupt, TTL: Parallel Port
Ref Clock sources:	IP CLK, 24 MHz Oscillator
Software Interface:	Control Registers, ID PROM, Vector Register, Status Ports
Initialization:	Hardware Reset forces all registers to 0 except the Vector Register which resets to 0XFF.
Access Modes:	Word in IO Space (see memory map) Word in ID Space Vectored interrupt
Access Time:	back-to-back cycles in 375ns (8MHz.) or 125ns (32 MHz.)
Wait States:	1 to ID space, INT, or IO space
Interrupt:	Transfer complete (Master) TTL Parallel Port – Up, Down, Change-of-State External Interrupt Change-of-State
DMA:	No Logic Interface DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	50-pin flat cable 50-screw terminal block interface User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max) inches
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/°C for uniform heat across IP
Power:	Max. 220 mA @ 5V



Order Information

IP-QuadUART-485-PLRA	IP Module with PLRA(Party Line Receiver), 16-bit IP interface Ground reference is DC coupled
Tools for IP-QuadUART-485-PLRA	IP-Debug-Bus - IP Bus interface extender http://www.dyneng.com/ipdbgbus.html IP--Debug-IO - IO connector breakout http://www.dyneng.com/ipdbgio.html
Eng Kit-IP-QuadUART-485-PLRA	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender Technical Documentation, 1. IP-QuadUART-485-PLRA Schematic 2. IP-QuadUART-485-PLRA Reference test software Data sheet reprints are available from the manufacturer's web site reference software.

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