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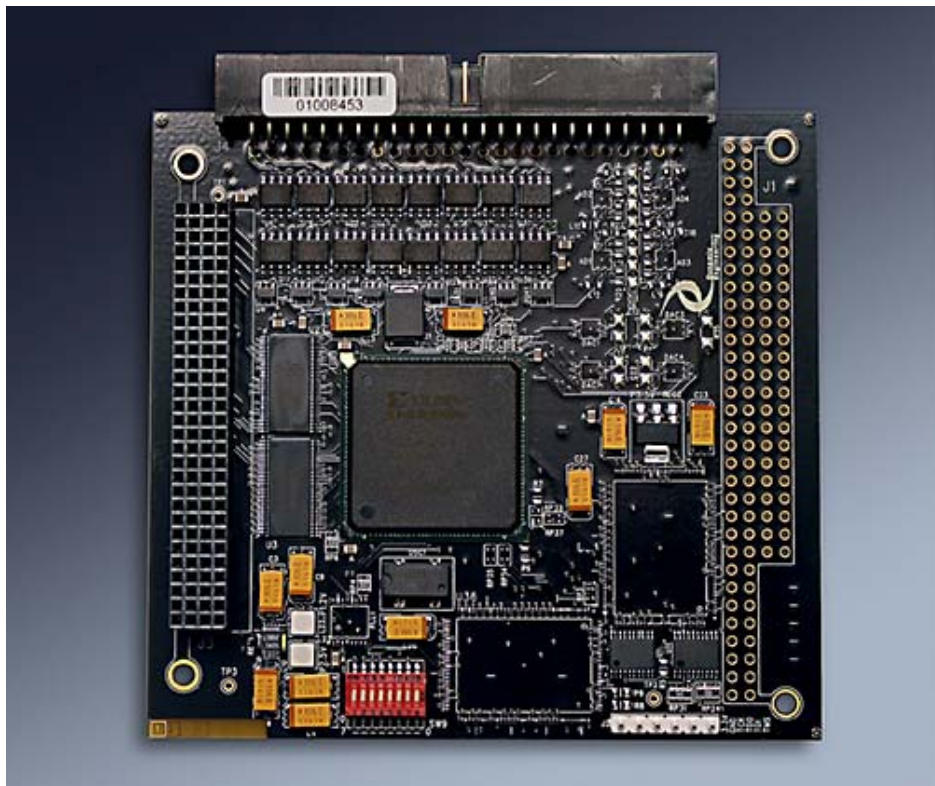
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User Manual

PC104p-BiSerial-III DDL

Digital Data-Link PC/104p Module



Revision B

Corresponding Hardware: Revision A

10-2006-0801

Corresponding Firmware: Revision B

PC104p-BiSerial-III DDL
Bi-Directional Serial Data Interface
PC/104p Module

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This product has been designed to operate with PC/104p Module stacks and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.



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Product Description

The PC104p-BiSerial-III is part of the PC/104p Module family of modular I/O components by Dynamic Engineering. The PC104p-BiSerial-III is capable of providing multiple serial protocols. The standard configuration shown in Figure 1 makes use of two external (to the Xilinx) FIFOs. The FIFOs can be as large as 128 k x 32-bits wide. Some designs do not require so much memory, and are more efficiently implemented using the Xilinx internal memory. The DDL protocol implemented provides two transmit and receive digital data-link channels each operating in either master or slave mode.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

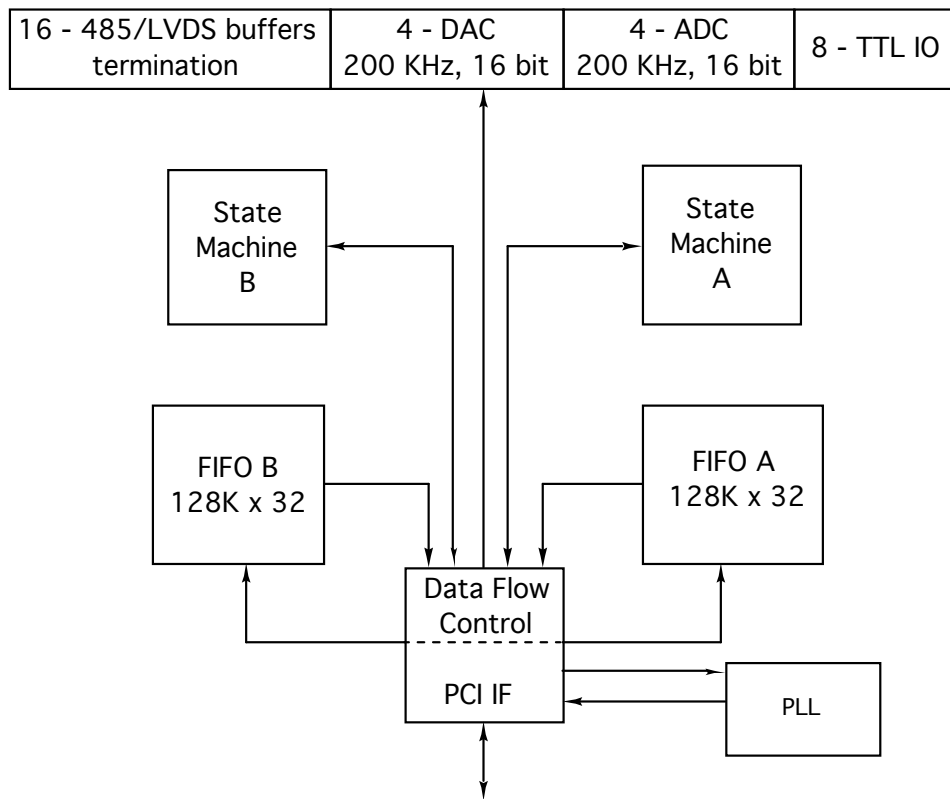


FIGURE 1

PC104P-BISERIAL-III BLOCK DIAGRAM

The DDL version is minimized and does not include the ADC, DAC, TTL or external FIFOs. Clock A from the PLL is used as an eight times clock reference for the DDL serial interfaces which transfer data at the rate of 100 k bits/second. Eight differential

I/O are used (four for each channel) for the I/O signals. The drivers and receivers conform to RS-485 (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 100Ω. The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. The terminations and transceivers are programmable through the Xilinx device to provide the proper mix of outputs, inputs and terminations needed for the DDL protocol implementation.

The DDL interface sends and receives 17-bit words (16 bits of data plus one parity bit) LSB first along with an active high enable signal and a gated clock (see figure 2 below). The data changes on the rising edge of the clock and is stable on the falling edge. The enable signal is asserted one bit period before the rising edge of the first clock and is de-asserted one bit period after the rising edge of the last clock. There is a programmable delay between data words that can be set from 1 to 255 bit periods. A parity bit is always appended to a data-word and can be set to use either odd or even parity.

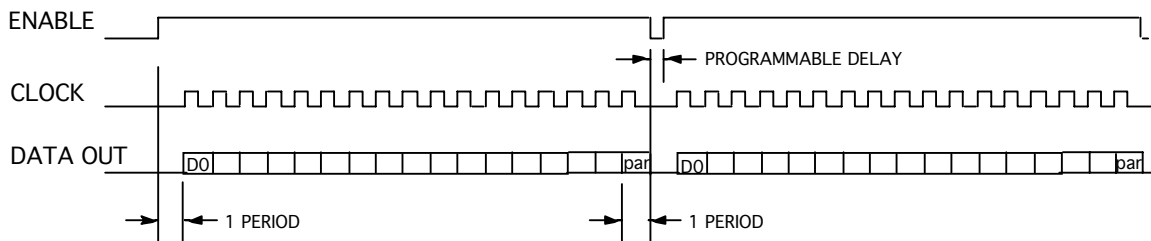


FIGURE 2 PC104P-BISERIAL-III DDL TIMING DIAGRAM

Similarly data is received in the same manner. The channel that is configured as the master drives the clock and enable signals for both data directions.

The DDL interface uses two 2k x 32-bit internal FIFOs for each channel, one each for the receiver and transmitter. 32-bit data is written to the transmit FIFO to be sent out least significant bit first. The lower 16-bit word is sent first along with a parity bit calculated from the data. The second word sent comes from the upper half of the FIFO word. This process continues until the FIFO is empty. If a message needs to contain an odd number of serial data-words, there is a control bit that will cause the last half of the last FIFO word to be discarded. When all transmit data has been sent, the transmitter can be configured to interrupt the host.

Similarly the receiver packs two data-words into each FIFO word until a pre-programmed word count is reached. If this count is an odd number, the upper half of the last FIFO word will be loaded with zeros before it is written to the receive FIFO. The receiver can also be configured to interrupt the host when this word count has been reached.

The transmitter and receiver can each be configured to operate in master or slave mode. A node in master mode is always connected to a node in slave mode. The definition of master mode is that this node drives the enable and clock signals and therefore also determines the inter-word gap delay value. The transmitter always drives the data signal and the receiver always receives the data, but the driver of the enable and clock depends on which node is in master mode. Also the I/O lines assigned to the transmitter and receiver are swapped when changing from master to slave mode and vice versa. This allows two channels to be connected with a straight across (pin-to-pin) cable.

Interrupts can also be configured to occur when the FIFOs reach programmable levels; almost empty for the transmitter and almost full for the receiver. All interrupts are individually maskable and a master interrupt enable is also provided to disable all interrupts on a channel simultaneously.

Scatter-gather DMA is supported with independent DMA engines for each transmitter and receiver. An arbiter controls bus access between the four DMA engines and priority can be given to any or all engines when FIFO levels reach their programmed limits in order to alleviate receiver overrun or transmitter under run.

The PC104p-BiSerial-III conforms to the PC/104p standard. This guarantees compatibility with multiple PC/104p boards. Because the PC/104p may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCI2PC104p – PCI carrier for PC/104p can be used for development in a conventional PC. Later the hardware and software can be ported to the target.

<http://www.dyneng.com/pci2pc104p.html>

Theory of Operation

The PC104p-BiSerial-III DDL is designed for transferring data from one point to another with a simple serial protocol.

The PC104p-BiSerial-III DDL features a Xilinx Spartan III FPGA. The FPGA contains all of the registers and protocol controlling elements of the PC104p-BiSerial-III design. Only the PLL, transceivers and switches are external to the Xilinx device in this design.

The PCI interface to the host CPU is controlled by a logic block within the Xilinx. The PC104p-BiSerial-III DDL design requires one wait state for read or writes to any address. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate with data state into the TRDY signal.

Scatter-gather DMA is provided for in this design with the memory page information stored in local RAM as a series of chaining descriptors. Once the physical address of the first chaining descriptor is written to the appropriate DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the I/O buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to a ‘1’ if this descriptor is the last in the chain. Bit one is set to a ‘1’ if the I/O transfer is from the PC104p-BiSerial-III DDL board to host memory, and a ‘0’ if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

With DMA the data is transferred at 33 MHz with 32-bit words for a transfer rate of 132 Mbytes/sec transfer rate when active. With most PC systems there is enough system overhead to reduce the effective transfer rate to approximately 50% of the maximum or 66 Mbytes/sec. With four channels running DMA (two in and two out) and 66 Mbytes/sec available there will be approximately 16.5 Mbytes/second available per channel. The DMA channels are independent allowing the data streams to be transferred to/from separate buffers in system memory with only the data flow controlling when the data is transferred, leaving the CPU available to do other processing tasks.

The clock A output from the PLL (CY22393) is used to synchronize transmitter and receiver operation and provide the serial timing reference when master mode is selected. The PLL is connected to the Xilinx by an I²C serial bus and uses a 40 MHz reference from the onboard oscillator and is programmed to generate 800 kHz for an eight times reference frequency. The PLL internal registers are loaded with 40 bytes of



data that are derived from a .jed file generated by the CyberClocks™ utility from Cypress semiconductor. Routines to program the PLL are included in the driver and UserApp code provided in the engineering kit for the board. This utility is available on our web site: <http://www.dyneng.com/CyberClocks.zip>. Note: When the driver initializes it will program the PLL to output the 800 kHz nominal frequency.

Transmit FIFO almost empty and receive FIFO almost full levels are programmable by writing values into the respective FIFO level registers. Besides generating FIFO level status and potentially causing an interrupt, these values are also be used to give DMA arbitration priority to a FIFO approaching its limit if enabled to do so. This process helps to prevent transmit FIFO under run and receive FIFO overrun when data is being transferred on more than one DMA channel. If a FIFO has reached its almost empty/full level, that FIFO will get priority in the DMA arbiter if its priority arbitration is enabled.

Address Map

Register Name	Offset	Description
PC104P_DDL_BASE_CNTRL	0x0000	// Base control register
PC104P_DDL_USER_SWITCH	0x0004	// User switch read port
PC104P_DDL_CNTRL_0	0x0010	// Control register
PC104P_DDL_STATUS_0	0x0014	// Status register
PC104P_DDL_FIFO_0	0x0018	// TX/RX FIFOs single word access
PC104P_DDL_WR_DMA_PNTR_0	0x001C	// Write DMA physical dpr address
PC104P_DDL_TX_FIFO_COUNT_0	0x001C	// Transmit FIFO data count
PC104P_DDL_RD_DMA_PNTR_0	0x0020	// Read DMA physical dpr address
PC104P_DDL_RX_FIFO_COUNT_0	0x0020	// Receive FIFO data count
PC104P_DDL_TX_AMT_0	0x0024	// Transmit FIFO almost empty level
PC104P_DDL_RX_AFL_0	0x0028	// Receive FIFO almost full level
PC104P_DDL_TX_CNTRL_0	0x002C	// Transmit configuration register
PC104P_DDL_RX_CNTRL_0	0x0030	// Receive configuration register
PC104P_DDL_TX_START_0	0x0034	// Transmitter start latch
PC104P_DDL_RX_START_0	0x0038	// Receiver start latch
PC104P_DDL_CNTRL_1	0x003C	// Control register
PC104P_DDL_STATUS_1	0x0040	// Status register
PC104P_DDL_FIFO_1	0x0044	// TX/RX FIFOs single word access
PC104P_DDL_WR_DMA_PNTR_1	0x0048	// Write DMA physical dpr address
PC104P_DDL_TX_FIFO_COUNT_1	0x0048	// Transmit FIFO data count
PC104P_DDL_RD_DMA_PNTR_1	0x004C	// Read DMA physical dpr address
PC104P_DDL_RX_FIFO_COUNT_1	0x004C	// Receive FIFO data count
PC104P_DDL_TX_AMT_1	0x0050	// Transmit FIFO almost empty level
PC104P_DDL_RX_AFL_1	0x0054	// Receive FIFO almost full level
PC104P_DDL_TX_CNTRL_1	0x0058	// Transmit configuration register
PC104P_DDL_RX_CNTRL_1	0x005C	// Receive configuration register
PC104P_DDL_TX_START_1	0x0060	// Transmitter start latch
PC104P_DDL_RX_START_1	0x0064	// Receiver start latch

FIGURE 3

PC104P BISERIAL-III DDL ADDRESS MAP

The address map provided is for the local decoding performed within the PC104p-BiSerial-III DDL. The addresses are all offsets from a base address, which is assigned by the system when the PCI bus is configured.

Programming

Programming the PC104p-BiSerial-III DDL requires only the ability to read and write data from the host. The base address of the module refers to the first user address for the slot in which the module is installed. This address is determined during system configuration of the PCI bus.

Depending on the software environment it may be necessary to set-up the system software with the PC104p-BiSerial-III DDL "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to receive data the software is only required to set the desired receiver configuration and start the receiver. To transmit the software will need to load the message into the transmit FIFO, set the desired configuration and enable the transmitter.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the interrupts on an individual basis. After the interrupt is received, the data can be retrieved. An efficient loop can then be implemented to fetch the data. New messages can be received even as the current one is read from the FIFO.

The transmit interrupt indicates to the software that a message has been sent and that the message has completed. If more than one interrupt is enabled, then the interrupt service routine (ISR) needs to read the status to see which source caused the interrupt. The interrupt status bits are latched, and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the ISR came from the current transfer.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

The VendorId = 0x10EE. The CardId = 0x0031.

Register Definitions

PC104P_DDL_BASE_CNTRL

[\$00] PC104p-BiSerial-III DDL Base Control Register (read/write)

Base Control Register	
DATA BIT	DESCRIPTION
31-20	Spare
19	PLL SDAT
18	PLL S2
17	PLL SCLK
16	PLL enable
15-8	Spare
7	Select disable
6-0	Spare

FIGURE 4 PC104P BISERIAL-III DDL BASE CONTROL REGISTER

Select disable: When '1' disables the two select bit latches that latch the state of user switch bits 0 and 1. These latches specify the position of the module in the PC104p stack (A-D) to route request, grant and interrupt signals. When these latches are disabled the user switch can be changed without affecting the stack configuration.

PLL enable: When this bit is set to a one, the PLL programming interface is enabled. When set to a zero, the interface is disabled.

PLL SCLK/SDAT: These signals are used to program the PLL over the I2C serial interface. SCLK is always an output whereas SDAT is bi-directional. When SDAT is to be read from the PLL, the SDAT bit in this register must be written high. This causes the SDAT output to be tri-stated allowing the SDAT line to be driven by the PLL. The state of the external SDAT line is read from the user switch port bit 19.

PLL S2: This is an additional control line to the PLL that can be used to select alternative pre-programmed frequencies.

The PLL is a separate device controlled by the Xilinx which has a fairly complex programming requirement. This can be greatly simplified by using the Dynamic Engineering driver to take care of the low-level bit manipulation requirements. Use the Cypress® CyberClocks utility to generate JEDEC files that specify the bit values of the PLL internal registers for requested frequencies.

PC104P_DDL_USER_SWITCH

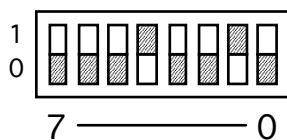
[\$04] PC104p-BiSerial-III DDL Switch Port / Design Revision (read only)

Design Revision/Switch port	
DATA BIT	DESCRIPTION
31-20	Spare
19	PLL SDAT input
18-16	Spare
15-8	Design revision
7-0	Switch 7-0

FIGURE 5

PC104P BISERIAL-III DDL USER SWITCH PORT

Switch 7-0: The Switch Read Port has the user bits. The user bits are connected to the onboard eight-position dipswitch. The switches allow custom configurations to be defined by the user. The software can identify a particular board by its switch settings in order to configure it accordingly.



The Dipswitch is marked on the silk-screen with the positions of the digits and the '1' and '0' definitions. The numbers are hex coded. The example shown would produce 0x12 when read.

Design revision: The current design revision for the DDL project is 0x01 (rev A). The revision will be updated as features are added or changes made.

PLL SDAT input: The SDAT line between the PLL and the Xilinx is bidirectional with an external 1 k Ω pull-up resistor. When the PLL SDAT bit in the Base Control Register is set to a one, the Xilinx SDAT output is tri-stated. The line can then be freely driven by the PLL device. The state of the external SDAT line is read from the read-only bit in this register.

PC104P_DDL_CNTRL_0, 1

[0x10, 0x3C] PC104p-BiSerial-III DDL Control Register (read/write)

Control Register	
DATA BIT	DESCRIPTION
31-14	Spare
13	I/O lines input termination enable
12	Master mode select
11	I/O lines output enable
10	Read DMA arbitration priority enable
9	Write DMA arbitration priority enable
8	Read DMA interrupt enable
7	Write DMA interrupt enable
6	Force interrupt
5	Master interrupt enable
4	Receive FIFO almost full interrupt enable
3	Transmit FIFO almost empty interrupt enable
2	FIFO test pass-through enable
1	Receive FIFO reset
0	Transmit FIFO reset

FIGURE 6

PC104P BISERIAL-III DDL CONTROL REGISTER

Transmit/Receive FIFO reset: When these bits are set to a one, the transmit and/or receive FIFOs will be reset. When these bits are zero, normal FIFO operation is enabled.

FIFO test pass-through enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO provided it is not full. This allows for fully testing the data FIFOs without using the I/O lines. When this bit is zero, normal FIFO operation is restored.

Transmit FIFO almost empty interrupt enable: When this bit is set to a one, the transmit FIFO almost empty interrupt is enabled. An interrupt will be asserted when the FIFO level becomes less than or equal to the count in the PC104P_DDL_TX_AMT register, provided the master interrupt enable is asserted. When this bit is zero, the transmit FIFO almost empty interrupt is disabled.

Receive FIFO almost full interrupt enable: When this bit is set to a one, the receive FIFO almost full interrupt is enabled. An interrupt will be asserted when the FIFO level becomes greater than or equal to the count in the PC104P_DDL_RX_AFL register, provided the master interrupt enable is asserted. When this bit is zero, the RX FIFO almost full interrupt is disabled.

Master Interrupt Enable: When this bit is set to a one, all enabled interrupts (except the DMA interrupts which operate independently) will be gated through to the host; when this bit is a zero, the interrupts can still be used for status without interrupting the host.

Force interrupt: When this bit is set to a one, a system interrupt will occur provided the master interrupt enable is set. This is useful to test interrupt service routines.

Write/Read DMA interrupt enable: When these bits are set to a one, the corresponding DMA channel interrupts are enabled. These interrupts occur when the current memory descriptor list for the corresponding scatter-gather DMA completes. The DMA interrupts are not affected by the Master Interrupt Enable.

Write / Read DMA arbitration priority enable: When these bits are set to a one, the corresponding DMA channel will get priority if it is near the limit of its FIFO (almost empty for the transmit FIFO or almost full for the receive FIFO). These limits are specified by the programmable counts in the PC104P_DDL_TX_AMT and PC104P_DDL_RX_AFL registers.

I/O lines output enable: When this bit is set to a one, the transmit data line and, when in master mode, the enable and clock lines will be active. When this bit is a zero, all the I/O output lines will be inactive. This allows for assigning Master/Slave status to connected channels without the I/O lines from both channels driving at the same time.

Master mode select: When this bit is set to a one, the channel is in master mode. This means that the local transmitter and receiver drive the enable and clock signals. When this bit is a zero, the channel is in slave mode and the enable and clock signals are driven by the remote transmitter and receiver.

I/O lines input termination enable: When this bit is set to a one, the receive data line and, when in slave mode, the enable and clock lines will be terminated. Each input line will be terminated with 100 Ω between the + and – sides of the differential pair. When this bit is a zero, the terminations will be inactive.

PC104P_DDL_STATUS_0, 1

[0x14, 0x40] PC104p-BiSerial-III DDL Status read/Latch clear write

Status Register	
DATA BIT	DESCRIPTION
31-24	Spare
23	Interrupt active
22-20	Spare
19	Read DMA error occurred
18	Write DMA error occurred
17	Read DMA interrupt occurred
16	Write DMA interrupt occurred
15-14	Spare
13	Receive FIFO almost full interrupt occurred
12	Transmit FIFO almost empty interrupt occurred
11	Spare
10	Receive parity error detected
9	Receive interrupt occurred
8	Transmit interrupt occurred
7	Receive data valid
6	Receive FIFO full
5	Receive FIFO almost full
4	Receive FIFO empty
3	Transmit data valid
2	Transmit FIFO full
1	Transmit FIFO almost empty
0	Transmit FIFO empty

FIGURE 7

PC104P BISERIAL-III DDL STATUS REGISTER

Transmit FIFO empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Transmit FIFO almost empty: When a one is read, the number of data words in the transmit data FIFO is less than or equal to the value written to the PC104P_DDL_TX_AMT register; when a zero is read, the FIFO level is more than this value.

Transmit FIFO full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Transmit data valid: When the transmitter is enabled or the FIFO test is enabled, the first word written to the transmit FIFO is read into a holding latch so that it will be immediately available. When this bit is read as a one, it signifies that this latch contains valid data. This bit can be set even if the transmit FIFO is empty. When this bit is a zero, it indicates that there is no valid transmit data in the holding latch.

Receive FIFO empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Receive FIFO almost full: When a one is read, the number of data words in the receive data FIFO is greater or equal to the value written to the PC104P_DDL_RX_AFL register; when a zero is read, the FIFO level is less than this value.

Receive FIFO full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Receive data valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO is empty, because as soon as the first four words are written into the FIFO, they are read out to fill the receive data pipe-line to be ready for a read DMA or single word access. When this bit is a zero, it indicates that there is no valid receive data remaining.

Transmit interrupt occurred: When a one is read, it indicates that the transmitter has sent at least one complete message since this bit was last cleared. A zero indicates that a new message has not been sent. This bit is latched and is cleared by writing back to the Status register with a one in this bit position.

Receive interrupt occurred: When a one is read, it indicates that the receive state-machine has received at least one complete message since this bit was last cleared. A message is complete when the number of received data-words equals the number in the word count field of the receiver control register. A zero indicates that a new message has not been received. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive parity error detected: When a one is read, it indicates that a parity error was detected in a received data-word. That is the received parity bit did not match the value calculated using the received 16 data-bits and the requested parity polarity. A zero indicates that no parity error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Transmit FIFO almost empty interrupt occurred: When a one is read, it indicates that the transmit FIFO has transitioned from greater than to less than or equal to the value in the PC104P_DDL_TX_AMT register. A zero indicates that the FIFO has not become almost empty. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive FIFO almost full interrupt occurred: When a one is read, it indicates that the receive FIFO has transitioned from less than to greater than or equal to the value in the PC104P_DDL_RX_AFL register. A zero indicates that the FIFO has not become almost full. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Write/Read DMA interrupt occurred: When a one is read, a write/read DMA interrupt is latched. This indicates that the scatter-gather list for the current write or read DMA has completed, but the associated interrupt has yet to be processed. A zero indicates that no write or read DMA interrupt is pending. These bits are latched and can be cleared by writing back to the Status register with a one in the appropriate bit position.

Write/Read DMA error occurred: When a one is read, a write or read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is incorrect. A zero indicates that no write or read DMA error has occurred. These bits are latched and can be cleared by writing back to the Status register with a one in the appropriate bit position.

Interrupt active: When a one is read, it indicates that an enabled user interrupt condition exists. A zero indicates that no enabled user interrupt condition exists. A user interrupt condition includes all interrupt sources that are controlled by the master interrupt enable i.e. all interrupts except the DMA interrupts. If the master interrupt enable is set, a system interrupt will be asserted if this status bit is also asserted.

PC104P_DDL_FIFO_0, 1

[0x18, 0x44] PC104p-BiSerial-III DDL Write TX/Read RX FIFO Port

RX and TX FIFO Port	
DATA BIT	DESCRIPTION
31-0	FIFO data word

FIGURE 8

PC104P BISERIAL-III DDL RX/TX FIFO PORT

This port is used to make single-word accesses into the transmit FIFO and out of the receive FIFO. This is useful for small data transfers.

PC104P_DDL_WR_DMA_PNTR_0, 1

[0x1C, 0x48] PC104p-BiSerial-III DDL Write DMA Pointer (write only)

Input DMA Pointer Address Register	
DATA BIT	DESCRIPTION
31-0	First chaining descriptor physical address

FIGURE 9

PC104P BISERIAL-III DDL WRITE DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather write DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer containing the data to write to the device, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

Note: Writing a zero to this port will abort a write DMA in progress.

PC104P_DDL_TX_FIFO_COUNT_0, 1

[0x1C, 0x48] PC104p-BiSerial-III DDL TX FIFO data count (read only)

TX FIFO Data Count Port	
DATA BIT	DESCRIPTION
31-12	Spare
11-0	Transmit data words stored

FIGURE 10

PC104P BISERIAL-III DDL TX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the transmit FIFO and data holding register (currently a maximum of 0x801).

PC104P_DDL_RD_DMA_PNTR_0, 1

[0x20, 0x4C] PC104p-BiSerial-III DDL Read DMA Pointer (write only)

Output DMA Pointer Address Register	
DATA BIT	DESCRIPTION
31-0	First chaining descriptor physical address

FIGURE 11

PC104P BISERIAL-III DDL READ DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather read DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer where the data from the device will be stored, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

Note: Writing a zero to this port will abort a read DMA in progress.

PC104P_DDL_RX_FIFO_COUNT_0, 1

[0x20, 0x4C] PC104p-BiSerial-III DDL RX FIFO data count (read only)

RX FIFO Data Count Port	
DATA BIT	DESCRIPTION
31-12	Spare
11-0	Receive data words stored

FIGURE 12

PC104P BISERIAL-III DDL RX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the receive FIFO and data pipeline (currently a maximum of 0x804).

PC104P_DDL_TX_AMT_0, 1

[0x24, 0x50] PC104p-BiSerial-III DDL Transmit FIFO almost-empty level (read/write)

Transmit FIFO Almost-Empty Level Register	
DATA BIT	DESCRIPTION
31-12	Spare
11-0	Transmit FIFO almost-empty level

FIGURE 13

PC104P BISERIAL-III DDL TX ALMOST EMPTY LEVEL REGISTER

This read/write port accesses the transmitter almost-empty level register. When the number of data words in the transmit data FIFO is equal or less than this value, the almost-empty status bit is set.

PC104P_DDL_RX_AFL_0, 1

[0x28, 0x54] PC104p-BiSerial-III DDL RX almost-full level (read/write)

RX Almost-Full Level Register	
DATA BIT	DESCRIPTION
31-12	Spare
11-0	RX FIFO almost-full level

FIGURE 14

PC104P BISERIAL-III DDL RX ALMOST FULL LEVEL REGISTER

This read/write port accesses the receiver almost-full level register. When the number of data words in the receive data FIFO is equal or greater than this value, the almost-full status bit is set.

PC104P_DDL_TX_CNTRL_0, 1

[0x2C, 0x58] PC104p-BiSerial-III DDL Transmitter Control Register (read/write)

Transmitter Control Register	
DATA BIT	DESCRIPTION
31-15	Spare
14	Send an odd number of words
13	Spare
12	Spare
11-4	Inter-word delay
3	Transmitter clear enable
2	Select odd parity
1	Transmit interrupt enable
0	Spare

FIGURE 15

PC104P BISERIAL-III DDL TRANSMITTER CONTROL REGISTER

Transmit interrupt enable: When this bit is set to a one, the transmit interrupt is enabled. A transmit interrupt will be asserted when the data written to the transmit FIFO has been completely sent, provided the master interrupt enable is asserted. When this bit is zero, the transmit interrupt is disabled.

Select odd parity: When this bit is set to a one, odd parity is used to determine the parity bit appended to the 16-bit serial data-word. This means that the number of ones in the 17 bits sent will be an odd number. When this bit is a zero, even parity is used.

Transmitter clear enable: When this bit is set to a one, the transmitter start latch will be cleared when the current message completes. When this bit is zero, the start latch will remain set until explicitly cleared.

Inter-word delay: This 8-bit field specifies the off-time of the enable signal between transmitted 17-bit words. This time is measured in transmit clock periods (nominally 10 microseconds) i.e. an inter-word delay of 10 would result in a gap of 0.1 milliseconds between words. This field is only applied when the transmitter is in master mode.

Send an odd number of words: Since the FIFO words are 32 bits and the serial data words are 16 bits, the number of data-words in the FIFO is implicitly an even number. If an odd length message is desired, this control bit should be set. When this bit is set to a one, only the lower half of the last FIFO word will be sent; the upper half of the FIFO word will be discarded. When this bit is a zero, both halves of the last word will be sent.

PC104P_DDL_RX_CNTRL_0, 1

[0x30, 0x5C] PC104p-BiSerial-III DDL Receiver Control Register (read/write)

Receiver Control Register	
DATA BIT	DESCRIPTION
31-16	Word count
15-12	Spare
11-4	Inter-word delay
3	Receiver clear enable
2	Select odd parity
1	Receiver interrupt enable
0	Spare

FIGURE 16

PC104P BISERIAL-III DDL RECEIVER CONTROL REGISTER

Receiver interrupt enable: When this bit is set to a one, the receive interrupt is enabled. If the master interrupt enable is asserted, a receive interrupt will occur, when the number of 16-bit data words received and stored in the receive FIFO equals the number in the word count field. When this bit is zero, the receive interrupt is disabled.

Select odd parity: When this bit is set to a one, odd parity is used to check the parity bit appended to the 16-bit serial data-word. This means that the number of ones in the 17 bits sent will be an odd number. When this bit is a zero, even parity is used. If the parity bit received does not match the calculated parity, the parity error status will be latched.

Receiver clear enable: When this bit is set to a one, the receiver start latch will be cleared when the specified word count is reached. When this bit is zero, the start latch will remain set until explicitly cleared.

Inter-word delay: This 8-bit field specifies the off-time of the enable signal between received 17-bit words. This time is measured in receive clock periods (nominally 10 microseconds) i.e. an inter-word delay of 10 would result in a gap of 0.1 milliseconds between words. This field is only applied when the receiver is in master mode.

Word count: This field represents the number of 16-bit data-words that will be received and stored in the receive FIFO. The first data-word is stored in the lower half of a FIFO word and the second data-word is stored in the upper half and the entire 32-bit word is written to the receive FIFO and so on. If this field is an odd number, the last 16-bit word will be stored in the lower half of the FIFO word, the upper half will be padded with zeros and the 32-bit word will be written to the FIFO. When the desired count is reached, an interrupt will occur provided the necessary enables are set. The receive start bit can also be cleared if that enable is set.

PC104P_DDL_TX_START_0, 1

[0x34, 0x60] PC104p-BiSerial-III DDL Transmitter Start Latch (read/write)

Transmitter Start Latch	
DATA BIT	DESCRIPTION
0	Transmit enable

FIGURE 17

PC104P BISERIAL-III DDL TRANSMITTER START LATCH

Transmit Enable: When this bit is a one the transmitter is enabled to send data-words. If the channel is in master mode, it will assert the enable I/O line and send clock and data to the remote receiver, provided data has been written to the transmit FIFO. If transmit data has not been written yet, data transmission will begin when the first word is written to the transmit FIFO. If the channel is in slave mode, the transmitter waits for the enable I/O line to be asserted and shifts data-bits out on the rising edge of the clock I/O line. If both the receiver and transmitter are enabled when the channel is in slave mode, the receiver has precedence and the transmitter will not start until the receive enable is cleared. When this bit is a zero the transmitter is disabled.

PC104P_DDL_RX_START_0, 1

[0x38, 0x64] PC104p-BiSerial-III DDL Receiver Start Latch (read/write)

Receiver Start Latch	
DATA BIT	DESCRIPTION
0	Receive Enable

FIGURE 18

PC104P BISERIAL-III DDL RECEIVER START LATCH

Receive Enable: When this bit is a one the receiver is enabled. If the channel is in master mode, it will assert the enable I/O line and send clocks to the remote transmitter. If the receiver is in slave mode it will wait for the enable I/O line to be asserted by the remote transmitter and shift data-bits in on the falling edge of the clock I/O line. In either case data-words will be received and stored in the receive FIFO until the requested word count has been reached. If both the receiver and transmitter are enabled when the channel is in master mode, the transmitter has precedence and the receiver will not start until the transmit enable is cleared. When this bit is a zero the receiver is disabled.

Interrupts

PC104p-BiSerial-III DDL interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with an interrupt the software must read the status register to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

For example, the PC104p-BiSerial-III DDL transmit state machine generates an interrupt request when a transfer is complete and the transmit interrupt enable and master interrupt enable bits are set.

The interrupt is mapped to INTA [or B or C or D based on the switch setting] on the PC/104p connector, which is mapped to a system interrupt when the PCI bus configures. The source of the interrupt is obtained by reading the status register. The status remains valid until that bit in the status register is explicitly cleared.

When an interrupt occurs, the master interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the latched bit and set the master interrupt enable bit high again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the status register. This allows for operating in polled mode simply by monitoring the status register.

Loop-back

The Engineering kit has reference software, which includes external loop-back tests which connect channel 0 to channel 1. The PC104p-BiSerial-III DDL uses a 50-pin ribbon cable connector for the I/O signals. The test requires an external cable with the following pins connected.

<u>SIGNAL</u>	<u>+</u>	<u>-</u>	<u>+</u>	<u>-</u>
Data1(TX/RX)	1	2	9	10
Clock	3	4	11	12
Enable	5	6	13	14
Data2(RX/TX)	7	8	15	16

Data1, Clock and Enable are outputs when the channel is configured as a Master and inputs when the channel is configured as a Slave. Data2 is an input when the channel is configured as a Master and an output when the channel is configured as a Slave. This allows two boards to be connected with a straight across cable when one is a Master and the other is a Slave.

PC104p-BiSerial-III DDL Header Pin Assignment

The figure below gives the pin assignments for the header connector on the PC104p-BiSerial-III design. Please note that the Analog and TTL IO are not installed on this version. GND* is a plane which is tied to GND through a 0805 0Ω resistor (DC coupling). AC coupling or open are options. For customized versions, or other options, contact Dynamic Engineering.

IO_0P TX/RX0 Data +	IO_0m TX/RX0 Data -	1	2
IO_1P Chan0 Clock +	IO_1m Chan0 Clock -	3	4
IO_2P Chan0 Enable +	IO_2m Chan0 Enable -	5	6
IO_3P RX/TX0 Data +	IO_3m RX/TX0 Data -	7	8
IO_4P TX/RX1 Data +	IO_4m TX/RX1 Data -	9	10
IO_5P Chan1 Clock +	IO_5m Chan1 Clock -	11	12
IO_6P Chan1 Enable +	IO_6m Chan1 Enable -	13	14
IO_7P RX/TX1 Data +	IO_7m RX/TX1 Data -	15	16
IO_8p	IO_8m	17	18
IO_9p	IO_9m	19	20
IO_10p	IO_10m	21	22
IO_11p	IO_11m	23	24
IO_12p	IO_12m	25	26
IO_13p	IO_13m	27	28
IO_14p	IO_14m	29	30
IO_15p	IO_15m	31	32
GND*	GND*	33	34
ADC0	TTL0	35	36
ADC1	TTL1	37	38
ADC2	TTL2	39	40
ADC3	TTL3	41	42
DAC0	TTL4	43	44
DAC1	TTL5	45	46
DAC2	TTL6	47	48
DAC3	TTL7	49	50

FIGURE 19

PC104P-BISERIAL-III CONNECTOR PINOUT

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard ribbon cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PC104p-BiSerial-III when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The PC104p-BiSerial-III does not contain special input protection. The connector is pinned out for a standard Header cable to be used. The wire pairs are defined to match up with the PC104p-BiSerial-III pin definitions. It is suggested that this standard cable be used for most of the cable run.

Custom cables can be manufactured with discrete wire header and direct connection to your mating equipment.

Terminal Block We offer a high quality 50-screw terminal block that directly connects to the ribbon cable. The terminal block can mount on standard DIN rails. HDRterm50 [<http://www.dyneng.com/HDRterm50.html>]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages.



Construction and Reliability

PC104p Modules are conceived and engineered for rugged industrial environments. The PC104p-BiSerial-III is constructed out of 0.062 inch thick High Temp FR4 material. The PC Boards are ROHS compliant. Dynamic Engineering has selected gold immersion processing to provide superior performance, and reliability (not subject to tin whisker issues).

The PC104p connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PC/104p device is secured into the stack with high insertion force pins and four screws attached to the 4 stand-offs. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PC/104p Module provides a low temperature coefficient of 1.7 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PC/104p. The coefficient means that if 1.7 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PC104p-BiSerial-III design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

<http://www.dyneng.com/warranty.html>

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is \$100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois, Suite 3
Santa Cruz, CA 95060
(831) 457-8891 - Fax (831) 457-4793
support@dyneng.com



Specifications

Host Interface:	PC/104p - 32 bit PCI bus
Serial Interface:	2 RX and 2 TX serial digital data-link ports.
Data rates generated:	100 kbits/sec
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses
Interrupt:	DMA read and write, TX and RX done, TX FIFO almost empty and RX FIFO almost full and Software interrupt for each channel.
DMA:	4 channel DMA, two TX and two RX.
Onboard Options:	All Options are Software Programmable
Interface Options:	50-pin ribbon cable or discrete wire 50-screw terminal block interface
Dimensions:	Standard Single PC/104p Module.
Construction:	FR4 Multi-Layer Printed Circuit, Surface Mount Components except connectors.
Temperature Coefficient:	1.7 W/°C for uniform heat across PC/104p
Power:	Max. TBD mA @ 5V

Order Information

PC104p-BiSerial-III DDL

PC104p Module with two bidirectional digital data-link channels, eight RS-485 I/O

Eng Kit-PC104p-BiSerial-III

HDRterm50 - 50 position screw terminal adapter

<http://www.dyneng.com/HDRterm50.html>

HDRcabl50 – 50 position ribbon cable

<http://www.dyneng.com/HDRribn50.html>

Technical Documentation,

1. PC104p-BiSerial-III Schematic
2. PC104p-BiSerial-III DDL Driver software and user application.

Data sheet reprints are available from the manufacturer's web site

Note: *The Engineering Kit is strongly recommended for first time PC104p-BiSerial-III purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. The revision letter is shown on the front of this manual as “Corresponding Hardware Revision.” This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.

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