

Reference page 32 of the Altera User Manual Revision H,

The TTL IO are designed with a '125 style gate, and read-back buffer. The '125 provides an "open drain" tri-state gate. The PCI-Altera-485/LVDS has a pull-up on each line. With revision H, and later hardware the enable for each '125 gate is tied to the Altera.

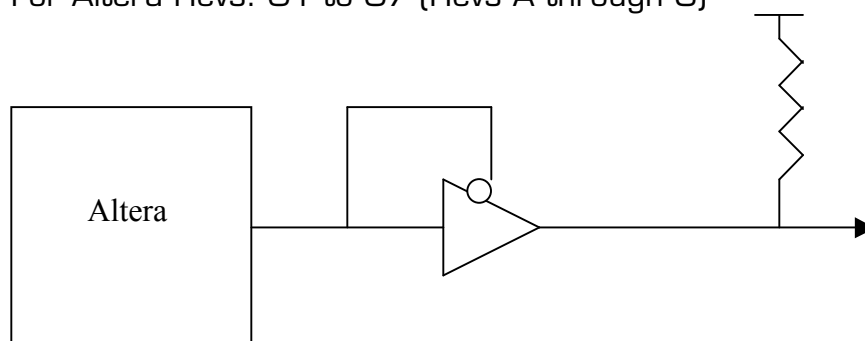
The default Engineering Kit VHDL design ties the enable to the data line for commonality with the previous versions. For users of previous revision boards wanting commonality with their previous implementation please tie the DATAEN[] to the DATA[] signal for each IO. The change will require a recompile of your VHDL.

For increased TTL switching performance; use the enables separately to leave the 125's always enabled to benefit from the high side current, and improved switch delay time compared to tri-state delay time.

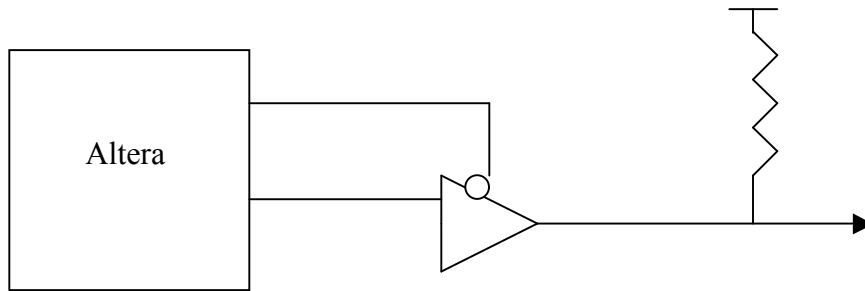
In the pre-revision H boards when the data is defined as a '0', the gate is enabled the corresponding line is pulled low. When the data is defined as a '1' the gate is disabled the line is pulled-high with the pull-up. With Revision H and later the enable can be left on utilizing the devices high side current to drive the signal high in addition to the pull-up action. The sense of the data will now follow the data line directly.

Below, are figures of what the configuration was before, and what it is now.

For Altera Revs. 01 to 07 (Revs A through G)



For Altera Rev. 08 (Revs H)



Below is the TTL enable pin out on the Altera FPGA Rev. 8 (Rev. H).

DATAEN[0]	L30	output	3.3-V PCI
DATAEN[1]	Y31	output	3.3-V PCI
DATAEN[2]	R2	output	3.3-V PCI
DATAEN[3]	N1	output	3.3-V PCI
DATAEN[4]	M1	output	3.3-V PCI
DATAEN[5]	T6	output	3.3-V PCI
DATAEN[6]	P2	output	3.3-V PCI
DATAEN[7]	K30	output	3.3-V PCI
DATAEN[8]	AD35	output	3.3-V PCI
DATAEN[9]	AC33	output	3.3-V PCI
DATAEN[10]	H30	output	3.3-V PCI
DATAEN[11]	J30	output	3.3-V PCI

To change back to the original TTL drive interface, add this code

```
DATAEN[X] <= TTL_Sig[X].
```

In the Altera FPGA code.