

DYNAMIC ENGINEERING

150 DuBois St Suite 3
831-457-8891 Fax 831-457-4793
sales@dyneng.com
www.dyneng.com
Est. 1988

User Manual

PMC-BiSerial-BAE1

Real Time Clock Data Interface PMC Module

Revision A2
Corresponding Hardware: Revision 1
10-2000-0101

PMC-BiSerial-BAE1
Real Time Clock Interface
PMC Module

Dynamic Engineering
150 DuBois St Suite 3
Santa Cruz, CA 95060
831-457-8891
www.dyneng.com

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Product Description

PMC-BiSerial is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-BiSerial is capable of providing multiple serial protocols.

Custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application. Several clocking options are available with the standard –IO version. The PMC Clock, 10 MHz. oscillator and external reference input are the clock sources. The source can be selected with software as can the divisor. A 12-bit counter is provided with a programmable divisor to offer a multitude of frequency options based on the three standard references. If a specific frequency is required that is not attainable with the standard choices we can install a “user” oscillator. Please be sure to select the proper source and clock divisors after reset to insure proper operation. Refer to the programming section for details.

Differential I/O is available on the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 130Ω. The resistors are in discrete 1206 packages to allow individual termination options for custom formats and protocols. There are 20 transceivers for the IO. The transceivers are programmable to allow more outputs or more inputs as needed for a specific protocol implementation.

The configuration implemented in the BAE1 uses four IO for Data 0, Clk 0, Data 1 and Clk 1. The pairs are used to transmit [master mode] or receive [target mode] RTC data. The mode and the termination are programmable. The RTC data is a 40 bit word plus command, framing and parity. In addition the target can respond to the command with “health check status” or a pre-programmed message.

All configuration registers support read and write operations for maximum software convenience. All addresses are long word aligned.

The PMC-BISERIAL conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software



compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

PMC-BiSerial uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors [height] to mate with the PMC-BiSerial, please let us know. We may be able to do a special build with a different height connector to compensate.

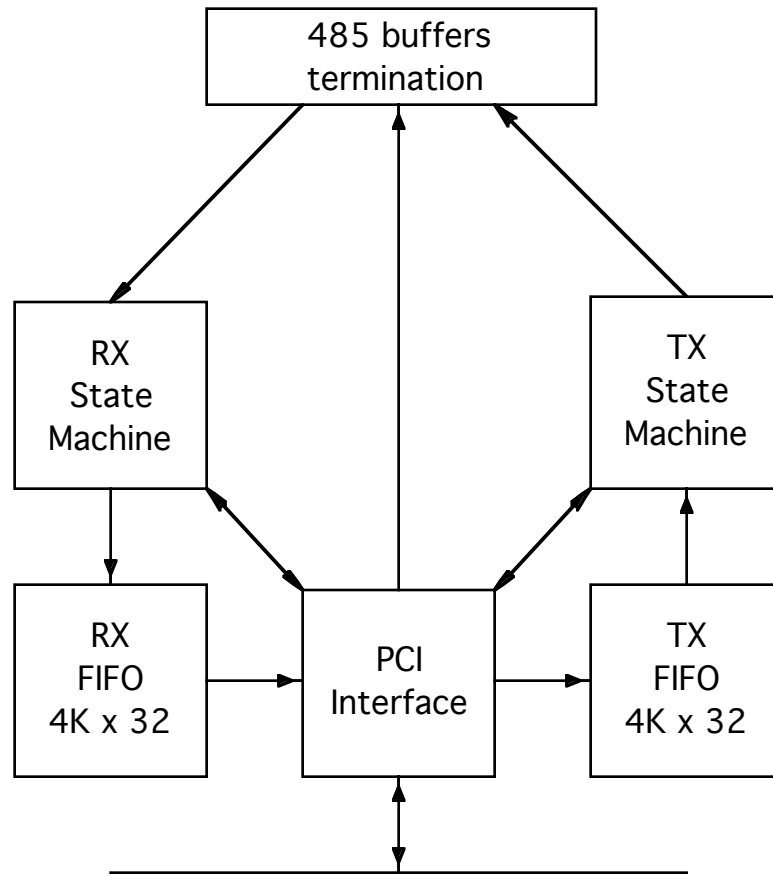


FIGURE 1

PMC-BISERIAL BLOCK DIAGRAM

The PMC-BiSerial-BAE1 implements an RTC interface protocol. Two channels are supported. Either channel can be a master or a target. If one channel is selected for master and one for target loop-back testing can be accomplished.

The design concept is to have a local 40 bit counter which the software can access. As a target; the counter is updated by the broadcast RTC value. The external clock is used to update the local timer and the broadcast value. The local timer “estimates” the RTC between updates from the master source. The software assigns an ID to the targets. All messages contain the RTC and all messages which pass parity checking are used to update the local counter. If the ID and Command match the local programmed values the target will respond to the master with either the ID and Command [health check] or a pre-programmed message.

If the –BAE1 is programmed to be a master then the process is somewhat reversed. The local counter becomes the system master. The reference is selected to be the local oscillator. The clock is broadcast to the targets along with the RTC values. The master keeps the time and repeats the broadcast every 128 uS [with a 2 MHz reference]. If the Master wants to check on a target then a command is embedded into the start of the message with the Target ID and Command to send. The Target will append data to the end of the message with the ID/CMD repeated or new data depending on the system configuration.

New messages are started with a “start bit” which is set to ‘1’. The next 8 bits are the ID [3] and Command[5]. 40 bits of RTC data follow. 5 parity bits correspond to the 5 bytes of RTC data are next. The stop bit is ‘0’. After the stop bit the master always releases the bus to allow the target to respond. If the master is not expecting a message then the message will be ignored. The sequence for the Target is turn-around, start = ‘1’ 8 bits of data, turn-around, then the master resumes driving the bus. Each of the subgroups are transmitted MSB first. Parity is programmable.

The master will drive the bus with ‘0’ between messages. The target uses a sequence of 64 ‘0’s to determine that the next ‘1’ is the start bit to protect against starting up mid-broadcast.

If the target does not detect a start bit an error flag is set and the target retries to synchronize. If the target is enabled before the master this condition should be expected until the master is on-line.

If the target detects parity errors the RTC value is not updated into the local counter. A status error bit is set when the status error is detected. If the data was valid then a status bit is set when the counter is updated.



When the master sends a command, the send command bit is automatically cleared by the Master state machine. When the target response is captured a status bit is set to indicate that a new message is stored.

All status bits are held until explicitly cleared by the system software.

The PMC-BiSerial design has 20 IO available. The base requirements use 4 IO. The remaining IO are fully programmable and can be used to transmit or receive RS-485 data through a simple register interface. The IO are programmable in groups of 4 for transmit or receive and termination. Each IO is independent for data.

The block diagram shows the FIFO built into the PMC BiSerial Base design. The PMC-BiSerial-BAE1 does not implement the FIFO interface within the Xilinx at this time. FIFO's are not installed. FIFO's can be added for your requirements. Please contact Dynamic Engineering for this option.



Theory of Operation

The PMC-BISERIAL is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design. In standard configuration, the PMC-BiSerial is a Type 1 mechanical with no components on the back of the board and one slot wide, with 10 mm inter-board height.

The PMC-BISERIAL-BAE1 is designed for transferring data from one point to another with a specific serial protocol. It features a Xilinx FPGA, which contains all of the registers and protocol controlling elements of the BISERIAL design. Only the transceivers, switches, and FIFOs are external to the Xilinx device.

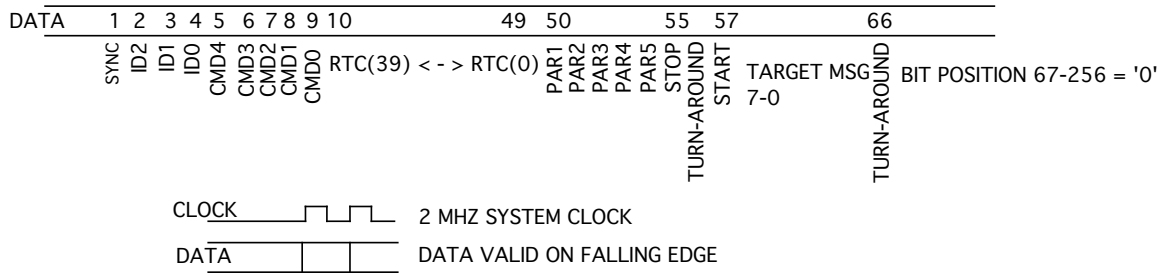
A logic block within the Xilinx controls the PCI interface to the host CPU. The BISERIAL design requires one wait state for read or write cycles to any address other than the FIFO loop-back ports, which require eight. The wait states refer to the number of clocks after the PCI core decode and before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate with data state into the TRDY signal.

The PMC-BISERIAL-BAE1 is designed to transmit and receive data using a broadcast RTC protocol. This protocol broadcasts RTC data every 128 uS over a serial bus. The PMC-BiSerial-BAE1 can transmit the data or receive the data through either of the two channels.

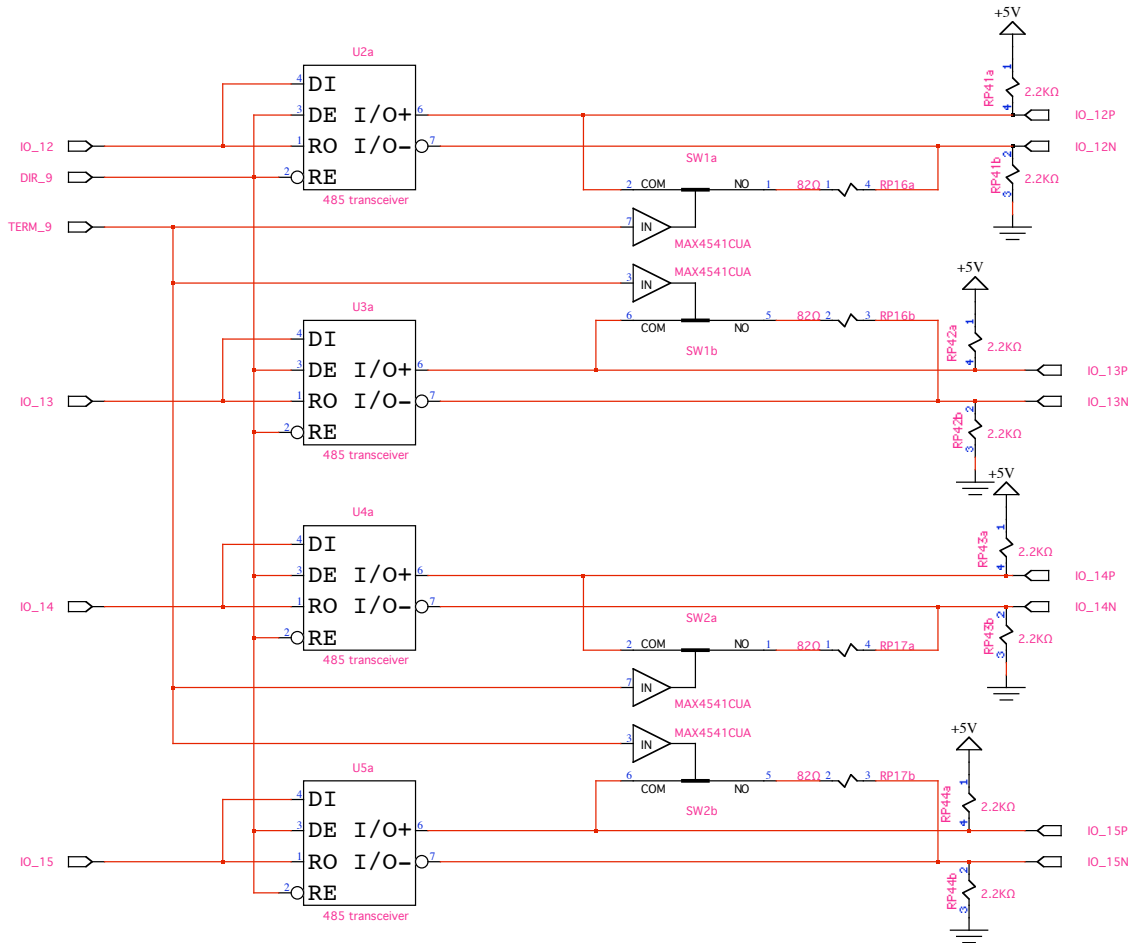
Clock reference sources include an on-board 16 MHz oscillator, the PCI clock and a user input clock. The oscillator is divided by 8 to provide a 50% duty cycle clock for Master mode. The external reference can be selected when acting as a target. Each channel is independent. Please refer to the memory map for more details.

The following timing diagram shows the bit positions of the broadcast data. The data is transmitted with the rising edge of the clock for both Master and Target and captured on the falling edge of the clock again for both Master and Target. The Xilinx makes use of the global buffers and edge registers to reduce skew and maximize data integrity.





The system clock is a 2 MHz reference. Data switches on the rising edge and is stable on the falling edge. The Parity is referenced to bytes within the RTC data. PAR1 is generated or check based on RTC 39-32, PAR2:31-24, PAR3:23-16, PAR4:15-8, PAR5:7-0.



There are 16 spare IO on the PMC-Parallel-BAE1. The 16 IO are arranged in four groups of 4 IO ea. Each group has separate direction and termination control via registers within the Xilinx. The IO are uncommitted and can be used for any user defined purpose. The IO are written to or read back via programmable registers. All of the read-back bits are always defined. The value will be the written value if the bits are set to be outputs or the bus side if defined to be inputs. The outputs will match the write register if defined to be outputs or the bus side if defined to be inputs.



Address Map

Function	Offset	function	Type
bis_base	EQU \$00	base control register	read/write
bis_pre_l	EQU \$04	preload RTC lower 7-0	read/write
bis_pre_u	EQU \$08	preload upper RTC 39-8	read/write
bis_cntl0	EQU \$0C	Control Channel 0	read/write
bis_cntl1	EQU \$10	Control Channel 1	read/write
bis_hmsg0	EQU \$14	health check received 0	read
bis_hmsg1	EQU \$18	health check received 1	read
bis_intc	EQU \$1C	undefined	read/write
bis_fifotx	EQU \$20	undefined	read/write
bis_fiforx	EQU \$24	undefined	read/write
bis_dir_term	EQU \$28	direction & termination	read/write
bis_RTC_u	EQU \$2C	read local RTC upper 39-8	read
bis_RTC_l	EQU \$30	read local RTC lower 7-0	read
bis_stat	EQU \$34	Status register	read/write
bis_rx_RTC_u	EQU \$38	read received RTC 39-8 ch 0	read
bis_rx_RTC_l	EQU \$3C	read received RTC 7-0 ch 0	read
bis_io	EQU \$40	IO data register	read/write

FIGURE 2

PMC-BISERIAL-BAE1 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the PMC-BiSerial-BAE1. The addresses are all offsets from a base address. The carrier board that the PMC is installed into provides the base address.

The VendorId = 0x10EE. The CardId = 0x0010. Current revision = 0x00



Programming

Programming the PMC-BISERIAL requires only the ability to read and write data from the host. The PMC Carrier board determines the base address. This documentation refers to the first user address for the slot that the PMC is installed in as the base address.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to receive data the software is only required to enable the channel 0 or channel 1 as a target, select the clock source and local RTC update source.

To operate as a master the local RTC value can be pre-loaded to a known value, the clock source selected and the channel enabled in the master mode.

The RTC value can be read at any time. The local counter is read when the data is required. The data width of the RTC is wider than the standard 32 bit PCI bus can accept in one read. The data read is captured from the RTC counter and held between reads to make sure that the values read are coherent. The data must be read upper then lower to insure proper operation.

On a periodic basis the software on a target system should read the status register and check that the error bits are not set and that the RTC loaded bit is set. The master may want to use the health check to see that the expected targets are on-line with the RTC communication.

The value to check against as a target is programmable. The ID of the card can be set allowing up to 8 PMC-Biserial-BAE1's to be used as targets in the same system plus another configured as a master. The command to compare against for the health check is also programmable to allow changes in the protocol to be accommodated easily.

A second message register is provided along with a control flag to substitute the message for the health check data when tasked by the master. A target to master communications link can be created by the master tasking the target to provide a response and the target responding when requested.



Register Definitions

All bits are active high and are reset on power-up or PCI reset. Undefined bits are unimplemented to save FPGA resources. Spare bits are implemented and have no defined function.

bis_base

\$00 BISERIAL Control Register Port read/write

Control Base	
DATA BIT	DESCRIPTION
31-29	spare
28	host load RTC [ld_rqst_p]
27	spare
26	odd_even
25-24	mselect
23-8	undefined
7-2	spare
1	clock select 1
0	clock select 0

FIGURE 3

PMC-BISERIAL-BAE1 BASE CONTROL REGISTER BIT MAP

When `ld_rqst_p` is set to '1' the local RTC will be preloaded with the value contained in the Pre-load Registers. The `mselect` must also be selected for PCI control for this bit to have effect. The system clock is used to sample the control bit which creates a requirement for this bit to be set for at least 500 nS before being cleared. Set – wait 500 nS+ - Clear. The RTC is loaded only once per active high `ld_rqst_p`. The control bit must be taken to '0' before re-loading the RTC. A 500 nS delay requirement also exists on the low time.

`Odd_even` is the selection bit for the parity generated and checked. '0' corresponds to even and '1' to odd parity. When even, the parity bit will be set or cleared to make the total number of bits in the byte plus parity bit even. For example: if there are 3 bits set in the byte then the parity bit will be set to make a total of 4 bits [even].

`Mselect` is used to select the source of the RTC preload value and the preload



request. “00” and “01” are the PCI port. “10” is channel 0. “11” is channel 1. The mux select should be configured to select the channel that data is being received on if the board is being used as a target and not a master. The mux should be configured to PCI if acting as a master. Channel 0 and channel 1 can be configured to be masters or targets independently. There is only one RTC counter. Channel 0 is the preferred target channel. Normally the hardware would not be configured as both a master and a target at the same time, but this configuration is useful for self-test. In this case the PCI bus should be selected for the mux.

Clock Select 0,1 are used to select where the reference clock originates for each channel and for the RTC. A combination of the Mselect and Clock selects affect the RTC. When ‘1’ the local oscillator is selected for that channel. When ‘0’ the external source is selected for that channel.

The RTC selection for reference clock is based on Mselect(0). When ‘0’ channel 0 clock is selected and when ‘1’ channel 1 is selected. If acting as a master then the RTC should be referenced to the local oscillator. The channel selected with Mselect(0) should be set to ‘1’ for the Clock Select bit. If acting as a target then the Mselect field should select the channel and the clock selector should be set to external for that channel. For Example Mselect = “10” and Clock Select 0 = ‘0’ to select channel 0 with the external reference.

bis_pre_l

\$04 BISERIAL Pre-load RTC Lower Port read/write

Control Pre-load Lower	
DATA BIT	DESCRIPTION
7-0	lower 8 bits of RTC pre-load data

FIGURE 4

PMC-BISERIAL-BAE1 LOWER PRE-LOAD BIT MAP

bis_pre_u

\$08 BISERIAL Pre-load RTC Upper Port read/write

Control Pre-load Upper	
DATA BIT	DESCRIPTION
31-0	upper 32 bits of RTC pre-load data

FIGURE 5

PMC-BISERIAL-BAE1 UPPER PRE-LOAD BIT MAP



The values contained in the Pre-load Registers will be loaded into the RTC if the Mselect is pointed to the PCI bus and a valid clock is selected when the Id_rqst_p signal is asserted.

bis_cntl0, bis_cntl1

\$0C/\$10 BISERIAL Control Register Channel 0/1 Port read/write

Control Channel 0,1	
DATA BIT	DESCRIPTION
31-24	msg_ch0/1
23-17	spare
16	msg_flag_0/1
15-8	id_cmd0/1
7-4	undefined
3	spare
2	master_target_0/1
1	enable_0/1
0	cmd_flg_0/1

FIGURE 6 PMC-BISERIAL-BAE1 CONTROL REGISTER CHANNEL 0/1 BIT MAP

Cmd_flag when '1' signals the master state machine that a command and address have been stored and are ready to be transmitted. The ID and Command will be transmitted on the next RTC broadcast. Once the ID and Command have been transmitted the cmd_flag will automatically be set to '0'. This flag only has meaning when acting as a master.

Enable when '1' turns on the state-machine for the associated channel. The type of operation should be selected first. The state-machine checks at the end of each operation to determine the type of operation to implement.

Master_target when '1' selects master mode operation. When a master the associated data IO line is driven allways except the target response window at the end of each broadcast RTC. The clock is always driven in master mode. In Target mode the hardware is configured to receive except when selected with the ID/CMD and at the appropriate window. The clock is always an input in target mode. The bis_dir_term register should be programmed to match for the clocks. The data bits are fully automatic.

Id_cmd is the field where the ID and Command are stored prior to setting the cmd_flg. The bits correspond to the RTC definition. MS 3 bits for the ID and the lower 5 for the command. The data is transmitted when in master mode and



compared against the incoming data in target mode.

The msg_flag is a secondary flag which is used by the target to respond with data other than the health check message when a matching id and command are received. The flag should be set when valid data is stored in the msg_ch(0,1) field and the master is expecting data other than the health check message. This flag only has meaning when acting as a target. The flag is automatically cleared when the data has been sent to the master. Please note that the master must initiate the transfer with a valid ID and Command.

Msg_ch is an alternate 8 bit field with data to use instead of repeating the id and command back to a master. The id_cmd or msg_ch data received by a [PMC-BiSerial-BAE1 is stored for access by the host computer.

bis_hmsg0, bis_hmsg1

\$14/\$18 BISERIAL health check message received [read only]

Data Bit	Status
7-0	received health check data from target

FIGURE 7 PMC-BISERIAL-BAE1 HEALTH CHECK MSG RECEIVED BIT MAP

The data received from an addressed target is stored into the bis_hmsg register. The data is over-written each time a target is queried and responds. A bit in the status register provides indication that the data is new and valid.

bis_dir_term

\$28 BISERIAL direction and termination Port [read/write]

Control DIRection and TERMination			
DATA BIT	DESCRIPTION		
7-0	DIRection	7-0	0 = read, 1 = drive
23-16	TERMination	7-0	1 = terminated

FIGURE 8 PMC-BISERIAL-BAE1 DIRECTION TERMINATION CONTROL BIT MAP

The direction for each of the 20 differential pairs is controlled through this port. The port defaults to '0' which corresponds to tri-stating the drivers.



Pull-up and Pull-down resistors built into some '485 interface devices may make the signal appear to be driven [if open] when in the tri-stated mode. Enabling the termination on a tristated line will yield approximately 2.5V on each side of the tri-stated driver.

The PMC-BISERIAL-BAE1 design uses the controlling state-machines to determine the the direction of IO1 and IO3. IO1 corresponds to channel 0 data and IO3 to channel 1 data. The clocks and the spare bits are controlled via the dir_term register.

<u>CONTROL</u>	<u>CORRESPONDING IO BIT(S)</u>
DIR0	Channel 0 Clock
DIR1	Channel 0 Data – state machine controlled
DIR2	Channel 1 Clock
DIR3	Channel 1 Data – state machine controlled
DIR4	IO_4..7
DIR5	IO_8..11
DIR6	IO_12..15
DIR7	IO_16..19

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others, it will make sense to use the onboard terminations.

The terminations for the receive groups should be set to terminate with the user software in most cases. Please note that the terminations are not under state-machine control.

<u>CONTROL</u>	<u>CORRESPONDING IO BIT(S)</u>
TERM0	Channel 0 Clock
TERM1	Channel 0 Data
TERM2	Channel 1 Clock
TERM3	Channel 1 Data
TERM4	IO_4..7
TERM5	IO_8..11
TERM6	IO_12..15
TERM7	IO_16..19



bis_RTC_u, bis_RTC_l

\$2C,\$30 BISERIAL RTC counter read Port [read]

Control RTC Local Read	
DATA BIT	DESCRIPTION
31-0	39-8 Upper read
31-24	7-0 Lower read
15-0	firmware revision [lower read]

FIGURE 9

PMC-BISERIAL-BAE1 RTC LOCAL READ BIT MAP

The local Real Time Clock can be read from this port pair. The RTC data is longer than the PCI data path width. It is important that the value read be from the same count for both parts of the 40 bit word. When the upper register is read the hardware captures the 40 bit word and holds it until the lower register is read. The RTC continues to count during the read process. It is important to read the data in the correct order. Reading out of order will causing unexpected results.

The firmware revision is currently 0x0000.

bis_stat

\$34 BISERIAL Status Port [read / write]

Data Bit	Status	
15	gnd	read '0'
14	clk0_error	'1' when external clock not active
13	gnd	read '0'
12	gnd	read '0'
11	frame_err1	1 = frame error on channel 1
10	frame_err0	1 = frame error on channel 0
9	par_err1	1 = parity error on channel 1
8	par_err0	1 = parity error on channel 0
7	undefined	unused
6	zero_cross	1 = counter has returned to '0'
5	no_data_rx1	1 = RTC data missing channel 1
4	no_data_rx0	1 = RTC data missing channel 0
3	rtc_id1	1 = RTC updated channel 1
2	rtc_id0	1 = RTC updated channel 0
1	h_msg1	1 = health message stored channel 1
0	h_msg0	1 = health message stored channel 0

FIGURE 10

PMC-BISERIAL-BAE1 STATUS BIT MAP

The status register is created out of two components. The status is captured from hardware conditions and held in the "Status Latch". Reading the status has no effect on the latch. Writing with a bit(s) set to the latch will clear the corresponding bit(s). The data bits corresponding to inactive or incorrect mode channels should be masked off. For example the health message flag for channel 1 should be ignored if channel 0 is used as the target.

CLK0_Error is set when the hardware detects that the clock received is not at the correct rate on channel 0. Due to hardware limitations there is no check on channel 1.

The detection circuit uses a state-machine to find the high to low transitions of the received clock. A counter uses the PCI clock to count from 0->1F then roll over. When the high to low transition of the input clock is detected the counter is reset. With a count of 0x1f the counter should not roll-over as it will be reset after 17 clocks. [33 MHz / 2 MHz] If the received clock stops then the counter will roll-over. A second circuit creates a pulse when the counter hits 0x1f.

Please note that a received clock which is too slow will have the same result as a non-existent clock. The transition detector prevents a stuck high or low clock from tricking the counter clearing mechanism. When changing the clock



reference control please allow 1 uS [once the dir_term register is programmed the delay can start.] or more for the received clock to be stable then clear the error condition. Once the clock is stable the error status should be cleared before using the status. Clear by setting bit 14 in the status register.

Frame_error(0,1) is set when in target mode and the received RTC stop bit is not set to '0'. The start bit is checked separately and would be reported as a "no data" error. Clear by setting the corresponding bit in the status register.

Par_err(0,1) is set when in target mode and the received RTC data has a parity error. The parity is generated by the target and checked against the parity received from the master. If the bits do not match then the error flag is set. Clear by setting the corresponding bit in the status register.

Zero_cross is set when the hardware detects that the local RTC has returned to the "0000000000" condition. Please note that this condition can be simulated by using the preset to get the RTC close to the roll-over value and then letting it run....better than waiting for 6 days to test. Clear the bit by setting bit 6 in the status register.

No_data_rx(0,1) is set when in target mode and the clock is running, but data is not received within the expected time frame. The RTC data is expected to be broadcast on a 128 uS period. If the target is enabled and the start bit is not detected within approximately 256 clocks an error is asserted. The state-machine first looks to see that the data is low for 64 clocks. When the low period has been satisfied the start bit is the next condition to check. In the loop checking for the start bit, the hardware keeps track of the number of clocks and aborts if too many accumulate before the start bit is detected. When the hardware aborts, the no_data error is asserted, and the state-machine returns to idle. The state-machine loop will retry until the software disables the channel or data becomes available. The error should be expected if the Target is started before the Master. The error is cleared by setting the corresponding bit in the status register.

RTC_Id(0,1) is set when in target mode and data has been received successfully. If the RTC data captured has good parity and is loaded into the local RTC then the bit is set. Clear by setting the corresponding bit in the status register.

H_msg(0,1) is set when in master mode and a health check message is received



from a target. The data is stored in the h_msg register. Clear by setting the corresponding bit in the status register.

bis_RX_RTC_u, bis_RX_RTC_l

\$38,\$3C BISERIAL Received RTC counter read Port [read]

Control RTC Local Read	
DATA BIT	DESCRIPTION
31-0	39-8 Upper read
7-0	7-0 Lower read

FIGURE 11

PMC-BISERIAL-BAE1 RTC RECEIVED BIT MAP

Data received through channel 0 [target mode] is captured once per 128 uS RTC broadcast period. The captured data is stored and then loaded into the local RTC. The local RTC should be accessed for the current “time” by the host software.

For test purposes it may be useful to have direct access to the data captured. The registers are not protected to the extent that the local RTC read-back is. Because the data is updated only once per 128 uS it is unlikely that the software will read the data while it is being updated. Please note that the lower 8 bits will be the same once the systems synchronize because the lower 8 bits correspond to 0xff which is 256 counts @ 500 nS each or 128 uS. The lower bits are real, but synchronized in such a way that they should be a “constant” from this port. The value will be different each time the hardware [master] is started because the delay from the counter pre-load to the master enable is variable. Restarting the target without changing the master will not change the lowest byte. The local counter is updated on a 500 nS basis instead of 128 uS period. The local counter will have changing data in the lowest byte.



bis_io

\$40 BISERIAL misc. IO Port [read/write]

Control RTC Local Read	
DATA BIT	DESCRIPTION
15-0	IO_19 – IO_4

FIGURE 12

PMC-BISERIAL-BAE1 IO PORT BIT MAP

The upper IO bits are available in a read-write port for user defined purposes. Each IO can be an input or an output on a nibble basis. The direction and termination is controlled via the `bis_dir_term` register. The bits when programmed to be outputs drive the IO. The port when read will report the state of the data bits directly before the transceivers. If the bits are programmed to be outputs then reading back will provide the written data. If the IO are programmed to be inputs then the read will provide the state of the IO received from an external source.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable with the following pins connected.

Clk+	1 – 4	IO0 – IO2
Clk-	35 - 38	
Data+	2 – 6	IO1 – IO3
Data-	36 - 40	

The upper 16 bits are looped back 8 on 8

IO4+ - IO12+	7 – 21 also connected to data+/-
IO4- - IO12-	41 – 55 when used with the no-data loop-back test
IO5+ - IO13+	9 - 22
IO5- - IO13-	43 - 56
IO6+ - IO14+	11 - 24
IO6- - IO14-	45 - 58
IO7+ - IO15+	12 - 26
IO7- - IO15-	46 - 60
IO8+ - IO16+	14 - 28
IO8- - IO16-	48 - 62
IO9+ - IO17+	16 - 30
IO9- - IO17-	50 - 64
IO10+ - IO18+	17 - 32
IO10- - IO18-	51 - 66
IO11+ - IO19+	19 - 34
IO11- - IO19-	53 – 68

The cable and HDEterm68 [without loop-back connections] are part of the engineering kit.

The PCI2PMC, PCIBPMC carrier cards can be used to mount the PMC-BiSerial-BAE1 in a standard PC using a PCI slot. We use this arrangement to perform the board level ATP. For system level debugging the PMC-Extendio provides the ability to remotely mount the PMC to the carrier via board and cable set.



PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BiSerial-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V[unused]	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 13

PMC-BISERIAL PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BiSerial-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V[unused]			1	2
			3	4
	GND		5	6
GND			7	8
			9	10
			11	12
RST#	BUSMODE3#		13	14
	BUSMODE4#		15	16
	GND		17	18
AD30	AD29		19	20
GND	AD26		21	22
AD24			23	24
IDSEL	AD23		25	26
	AD20		27	28
AD18			29	30
AD16	C/BE2#		31	32
GND			33	34
TRDY#			35	36
GND	STOP#		37	38
PERR#	GND		39	40
	SERR#		41	42
C/BE1#	GND	43		44
AD14	AD13		45	46
GND	AD10		47	48
AD8			49	50
AD7			51	52
			53	54
	GND		55	56
			57	58
GND			59	60
			61	62
GND			63	64

FIGURE 14

PMC-BISERIAL PN2 INTERFACE

BiSerial-BAE1 Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-BiSerial. Also, see the User Manual for your carrier board for more information. GND* is a plane which is tied to GND through a 1206 0Ω resistor. AC or open are options – contact Dynamic Engineering.

IO_0p [clk0+]	IO_0m [clk0-]	1	35
IO_1p [data0+]	IO_1m[data0-]	2	36
GND*	GND*	3	37
IO_2p[clk1+]	IO_2m [clk1-]	4	38
GND*	GND*	5	39
IO_3p [data1+]	IO_3m [data1-]	6	40
IO_4p	IO_4m	7	41
GND*	GND*	8	42
IO_5p	IO_5m	9	43
GND*	GND*	10	44
IO_6p	IO_6m	11	45
IO_7p	IO_7m	12	46
GND*	GND*	13	47
IO_8p	IO_8m	14	48
GND*	GND*	15	49
IO_9p	IO_9m	16	50
IO_10p	IO_10m	17	51
GND*	GND*	18	52
IO_11p	IO_11m	19	53
GND*	GND*	20	54
IO_12p	IO_12m	21	55
IO_13p	IO_13m	22	56
GND*	GND*	23	57
IO_14p	IO_14m	24	58
GND*	GND*	25	59
IO_15p	IO_15m	26	60
GND*	GND*	27	61
IO_16p	IO_16m	28	62
GND*	GND*	29	63
IO_17p	IO_17m	30	64
GND*	GND*	31	65
IO_18p	IO_18m	32	66
GND*	GND*	33	67
IO_19p	IO_19m	34	68

FIGURE 15

PMC-BISERIAL FRONT PANEL INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC-BiSerial Module routed to Pn4. Also, see the User Manual for your carrier board for more information.

IO_0p	clk0+	IO_0m	clk0-	1	2
IO_1p	data0+	IO_1m	data0-	3	4
IO_2p	clk1+	IO_2m	clk1-	5	6
IO_3p	data1+	IO_3m	data1-	8	9
IO_4p		IO_4m		9	10
IO_5p		IO_5m		11	12
IO_6p		IO_6m		13	14
IO_7p		IO_7m		15	16
IO_8p		IO_8m		17	18
IO_9p		IO_9m		19	20
IO_10p		IO_10m		21	22
IO_11p		IO_11m		23	24
IO_12p		IO_12m		25	26
IO_13p		IO_13m		27	28
IO_14p		IO_14m		29	30
IO_15p		IO_15m		31	32
IO_16p		IO_16m		33	34
IO_17p		IO_17m		35	36
IO_18p		IO_18m		37	38
IO_19p		IO_19m		39	40
				41	42
				43	44
				45	46
				47	48
				49	50
				51	52
				53	54
				55	56
				57	58
				59	60
				61	62
				63	64

FIGURE 16

PMC-BISERIAL-BAE1 PN4 INTERFACE

Applications Guide

Interfacing

The pinout tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC-BiSerial when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. PMC-BISERIAL does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the BiSerial pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68 screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68

[<http://www.dyneng.com/HDEterm68.html>]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages.



Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BiSerial is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BISERIAL design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.



Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

<http://www.dyneng.com/warranty.html>

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is \$100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite 3
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com



Specifications

Host Interface:	PCI Mezzanine Card
Serial Interface:	RS-485 CLK0, DATA0,CLK1,DATA1
Parallel Interface	RS-485 16 bits with programmable direction and termination
TX CLK rates generated:	2 MHz local and input clock(s)
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/°C for uniform heat across PMC
Power:	Max. TBD mA @ 5V



Order Information

PMC-BISERIAL-IO-BAE1	PMC Module with two RTC data channels, Special protocol support Master and Target Modes, RS-485 drivers and receivers 32 bit data interface
Eng Kit–PMC-BISERIAL-BAE1	HDEterm68 - 68 position screw terminal adapter HDEcabl68 - 68 IO twisted pair cable Technical Documentation, 1. PMC-BISERIAL Schematic 2. PMC-BISERIAL-BAE1 Reference test software Data sheet reprints are available from the manufacturer's web site reference software.
Other Support	The PCI2PMC, PCIBPMC carrier cards can be used to mount the PMC-BiSerial-BAE1 in a standard PC using a PCI slot. We use this arrangement to perform the board level ATP. For system level debugging the PMC- Extendio provides the ability to remotely mount the PMC to the carrier via board and cable set.

Note: *The Engineering Kit is strongly recommended for first time PMC-BISERIAL buys.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.

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