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User Manual

PMC-BiSerial

Version PS1

Bi-directional Serial Data Interface PMC Module

Revision A
Corresponding Hardware: Revision A

PMC-BiSerial-PS1
Bi-directional Serial Data Interface
PMC Module

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Product Description

PMC-BiSerial-PS1 is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-BiSerial-PS1 is a special version of the BiSerial. Four Transmit channels are available in this version. Channel 0 is the standard transmit channel altered for LSB first data. Channels 1-3 utilize internal FIFOs [4 x 32] and a fixed sync pattern [0x7FFFFFFF].

Please contact Dynamic Engineering with your custom application.

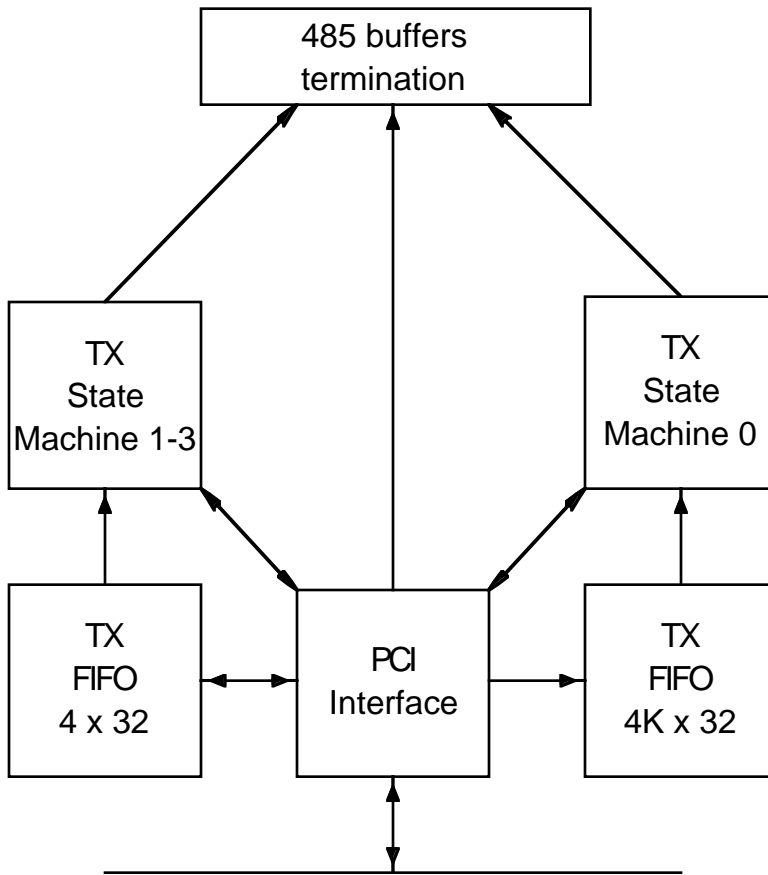


FIGURE 1

PMC-BISERIAL-PS1 BLOCK DIAGRAM

Several clocking options are available with the standard -IO version. The



-PS1 version is preset to 5 MHz. for the transmit rate.

Differential I/O is available on the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 130Ω . The resistors are in discrete 1206 packages to allow individual termination options for custom formats and protocols. There are 20 transceivers for the IO. The transceivers are programmable to allow more outputs or more inputs as needed for a specific protocol implementation. The standard configuration is Data, Clock, and Strobe for Receive and Transmit plus a reference clock input. The transceivers are programmed through the Xilinx device for maximum flexibility. The terminations are also programmable to be active or not. The -PS1 has an additional 3 transmit channels defined on IO 8-10.

All configuration registers support read and write operations for maximum software convenience. All addresses are long word aligned.

The PMC-BISERIAL conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

PMC-BiSerial uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors [height] to mate with the PMC-BiSerial, please let us know. We may be able to do a special build with a different height connector to compensate.

Serial channel 0 is supported by an external [to the FPGA] 4K by 32 bit FIFO. The FIFO supports long word reads and writes. Serial channels 1-3 are supported with 4 x 32 FIFOs implemented within the FPGA. A path exists for loop-back testing of the internal FIFO. The PMC data path is 32 bits wide. The design is optimized for the system configuration with minimal delay on the PCI write to TX FIFO path.

Data is sent LSB first. Data is sent when the transmitter is enabled and data is stored within the FIFO. Transmission completes when the FIFO is detected to be empty for channel 0 and after the 4 words are sent for channels 1-3. The Strobe signals that data is active on the serial data output for channel 0. Channels 1-3 do not have a strobe reference. The



strobe is active low. The strobe and data switch on the falling edge and are valid on the rising edge of the TX clock.

Smaller and larger FIFOs are available as a special order.

Interrupts are supported by the PMC-BISERIAL. The interrupt occurs at the end of the message. The interrupts are individually maskable. The interrupt occurs on INTA. The FIFO status is available for the FIFO making it possible to operate in a polled mode. In addition to the protocol interrupts there are interrupts associated with the programmable FIFO flags. The Programmable Almost Empty flag is used with the transmitter to allow software to operate in an interrupt driven mode and to keep the TX FIFO from going empty.



Theory of Operation

The PMC-BISERIAL is designed for transferring data from one point to another with a serial protocol.

The PMC-BISERIAL features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BISERIAL design. Only the transceivers, switches, and channel O FIFOs are external to the Xilinx device.

The PMC-BISERIAL is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design. In standard configuration, the PMC-BiSerial is a Type 1 mechanical with no components on the back of the board and one slot wide, with 10 mm inter-board height.

The PCI interface to the host CPU is controlled by a logic block within the Xilinx. The BISERIAL design requires one wait state for read or write cycles to any address. The PMC-BISERIAL is capable of supporting 40 MBytes per second into and out of the FIFOs. The wait states refer to the number of clocks after the PCI core decode before the "terminate with data" state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate with data state into the TRDY signal.

The serial I/O can support many protocols. The -PS1 timing is shown in the next diagram. The clock is free running, the data is valid on the rising edge of the clock, and strobe frames the data for channel O.

State machines within the FPGA control all transfers between the FIFO and FPGA, and the FPGA and the data buffers. The TX state machine reads from the transmit FIFOs and loads the shift registers before sending the data.

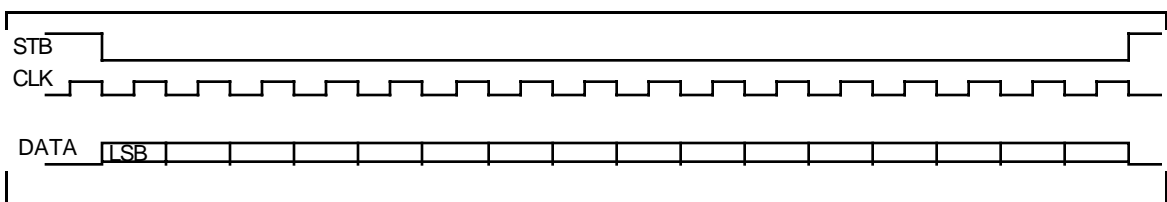


FIGURE 2

PMC-BISERIAL-PS1 SERIAL PROTOCOL TIMING



Data is read from the TX FIFO and loaded into the shift register. The LSB is then present at the output of the data buffer. The Strobe is activated at the same time. One half clock period later the rising edge of the data clock is driven to the output clock buffer. One half clock period later, the data is transitioned to the next value. The LSB+1 is now on the data lines. The process repeats until the first word is transferred. In Channel 0 if the FIFO is not empty from reading the first word then the process repeats for the second word. There are no inter-word gaps. The data stream is continuous from LSB to MSB for a compact serial transfer. The first word written to the FIFO serves as the Sync Pattern for this implementation.

In Channels 1-3 the FIFO is smaller and fixed. When the transmitter is enabled a fixed synchronization pattern is transmitted then 4 words from the FIFO.

When the transmission is complete the Transmit enable bit is cleared and an interrupt, if enabled, is generated. Transfer is fixed at 5 MHz with the BiSerial-PS1 design.



Address Map

Function	Offset	function	Type
bis_base	EQU \$00	base control register	read/write
bis_tx	EQU \$04	transmit base control	read/write
bis_txs	EQU \$08	unimplemented	read/write
bis_rx	EQU \$0c	unimplemented	read/write
bis_rxs	EQU \$10	unimplemented	read/write
bis_STAT0	EQU \$14	status register 0	read
bis_STAT1	EQU \$18	status register 1	read
bis_intc	EQU \$1C	interrupt clear	write
bis_fifotx	EQU \$20	transmit FIFO access	read/write
bis_fiforx	EQU \$24	unimplemented	read/write
bis_dir_term	EQU \$28	direction & termination	read/write
bis_fifo1	EQU \$2C	internal FIFO channel 1	read/write
bis_fifo2	EQU \$30	internal FIFO channel 2	read/write
bis_fifo3	EQU \$34	internal FIFO channel 3	read/write
bis_switch	EQU \$44	unimplemented	read

FIGURE 3

PMC-BISERIAL-PS1 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the PMC-BiSerial. The addresses are all offsets from a base address. The carrier board that the PMC is installed into provides the base address.

The VendorId = 0x10EE. The CardId = 0x0006. Current revision = 0x00



Programming

Programming the PMC-BISERIAL requires only the ability to read and write data from the host. The base address is determined by the PMC Carrier board.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial "registration" data. For example in WindowsNT there is a system registry which is used to identify the resident hardware.

In order to receive data the software is only required to enable the RX state machine and FIFOs. If desired, the interrupt can be enabled and parity selected. Data will be loaded into the FIFOs as it is received.

The interrupt service routine should be loaded and the mask should be set.

The end of transmission interrupt will indicate to the software that the message has been started and that the message has terminated. If the TX interrupts are enabled then the SW needs to read BIS_STATO to see which source caused the interrupt. Reading BIS_STATO will clear the interrupt status and accessing BIS_INTC will clear the actual interrupt. It is a good idea to read the status register to force the TX_INT bits to zero before Start is enabled. This will insure that the TX_INT=1 value read by the interrupt service routine came from the current reception.

Before transmitting data, the FIFOs are enabled and the data loaded. Once the complete message is loaded and the controls set properly the start bit can be set to cause the transfer to begin. When the TX interrupt is received the transmission has been completed and another message can be loaded. All that needs to happen with a second message is to load the FIFO and set the start bit.

Messages longer than 16K bytes can be accommodated by special ordering HW with larger FIFOs, by polling or using the programmable flag interrupts. To poll read the Status O register during the transfer and take appropriate action when the full, empty or programmable flag shows that there is data to read or space to write. The PAE flag is implemented to provide an almost empty interrupt to allow the TX side to operate in an interrupt driven mode with longer messages.



Register Definitions

bis_base

\$00 BISERIAL Control Register Port read/write

CONTROL BASE	
DATA BIT	DESCRIPTION
31-23	spare
22	FRX_LD
21	FTX_LD
20	FIFO_EN
19-18	spare
17	INT_SET
16	INT_EN_MASTER
15-0	spare

FIGURE 4

PMC-BISERIAL-PS1 BASE CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

FRX_LD is tied to the RX FIFO WE2/_LD pin. FTX_LD is tied to the TX FIFO WE2/_LD pin. When the FIFOs are taken out of reset it is possible to set-up the FIFO to accept commands to program the way the programmable almost empty and programmable almost full signals operate. ***In the standard transfer mode these pins are set hi before FIFO_EN is set to use as a second WE control pin.*** If the PAE and PAF flags are used then the FIFOs will require programming.

FIFO_EN when '1' takes the FIFO out of reset. To create a reset be sure to leave in the '0' state for the reference clock to capture the reset. This can be an issue if a slow transmission rate is chosen. To guarantee reset the PCI clock can be used as a reference for both the TX and RX FIFOs temporarily then set back to the original settings.

INT_SET is used for test and software development purposes to create an interrupt request. 1 = assert interrupt request. 0 = normal operation. Useful to stimulate interrupt acknowledge routines for development.

INT_EN_MASTER when '1' gates all interrupts through to the PCI host. When '0' the interrupts can be used for status without interrupting the host.



bis_tx

\$04 BISERIAL TX Control Register Port read/write

CONTROL TX	
DATA BIT	DESCRIPTION
31-10	spare
9	clock en
8	int_en_pae
7	int_en_tx3
6	int_en_tx2
5	int_en_tx1
4	int_en_tx0
3	start_tx3
2	start_tx2
1	start_tx1
0	start_tx0

FIGURE 5

PMC-BISERIAL-PS1 TX CONTROL REGISTER BIT MAP

Clock_en when '1' gates the transmit clock to be driven to TX_CLK. The gate is provided to allow FIFO loop back testing without driving the clock onto the transmission line. When '0' the TX_CLK is held in at '0'. The enable should normally be set.

INT_EN_TX0-3 is the Interrupt Enable bit for the Transmit channel. The default state is off. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the transmission is complete. The interrupt is cleared by writing to bis_intc.

INT_EN_PAE = 1 to enable the FIFO Programmable Almost Empty interrupt. When enabled an interrupt is generated when the data level falls to the programmed level. The interrupt is cleared by reading the status register [bis_stat0]

Start_tx0-3 when set will start a transmission. Start_TX0-3 is auto-cleared when the transmission is complete. Start_TX0-3 are designed to be write '1' only, clear via end of transmission, with read-back. Test and set of the lower bits is un-necessary.



bis_txs

\$08 BISERIAL TX Special Control Register Port read/write

CONTROL TX Special	
DATA BIT	DESCRIPTION
31-0	unimplemented

FIGURE 6 PMC-BISERIAL-PS1 TX SPECIAL CONTROL REGISTER BIT MAP

bis_rx

\$0C BISERIAL RX Control Register Port read/write

CONTROL RX	
DATA BIT	DESCRIPTION
31-0	unimplemented

FIGURE 7 PMC-BISERIAL-PS1 RX CONTROL REGISTER BIT MAP

bis_rxs

\$10 BISERIAL RX Special Control Register Port read/write

CONTROL RX Special	
DATA BIT	DESCRIPTION
31-0	unimplemented

FIGURE 8 PMC-BISERIAL-PS1 RX SPECIAL CONTROL REGISTER BIT MAP



bis_stat0

[\$14] BISERIAL Status Port [read only]

Data Bit	Status	
15	tx_int3	1 = tx3 int rqst
14	tx_int2	1 = tx2 int rqst
13	tx_int1	1 = tx1 int rqst
12	fae_int	1 = programmable almost empty int rqst
11	tx_int0	1 = tx0 int rqst
10	ftx_ffn	0 = tx fifo full 1 = not full
9	ftx_faen	0 = almost empty 1 = not almost empty
8	ftx_mtn	0 = tx fifo empty, 1 = not empty
7	int_request	1 = interrupt request after int_en mask
6-0	unused	test only mask off

FIGURE 9

PMC-BISERIAL-PS1 STATUS REG 0 BIT MAP

The FIFO flags are active low. When the empty bit is low then the FIFO is empty. When the empty flag is high then the FIFO has at least one piece of data stored. When the Full Flag is set [low] the FIFO is full. When not set then the FIFO still has room.

When int_request is set then the at least one of the maskable interrupts is active and the master enable is set to allow interrupts.

Tx_int when set indicates that the transmission has completed. To clear, write to bis_intc with any pattern. The status bit is a separate registered version of the interrupt request. The status bit is cleared when the status register is read. If the interrupt request has not been cleared then the status will become set again because the request is still present. Once the bis_intc has been written to, the interrupt will clear, and the status read will clear and stay cleared. An alternate method of clearing the tx_int is to disable the interrupt enable for TX0-3.



bis_stat1

[\$18] BISERIAL Status Port [read only]

Data Bit	Status
15-0	unimplemented

FIGURE 10

PMC-BISERIAL-PS1 STATUS REG 1 BIT MAP

bis_intc

[\$1c] BISERIAL Interrupt Clear Port

The user can, by accessing this port, cause the BISERIAL to clear the pending interrupt requests. Any data pattern can be written.

bis_fifotx

[\$20] BISERIAL TX FIFO write only port

The BISERIAL supports 32 bit writes to the transmit data FIFOs. Data is aligned D31-0. This port is only written to.

bis_fiforx

[\$24] BISERIAL RX FIFO write-read port
unimplemented in the -PS1 design

bis_dir_term

[\$28 BiSerial direction and termination Port read/write]

CONTROL REGISTER DIR_TERM	
DATA BIT	DESCRIPTION
7-0	DIRection 7-0 0 = read, 1 = drive
23-16	TERMination 7-0 1 = terminated

FIGURE 11

PMC-BISERIAL-PS1 DIRECTION TERMINATION CONTROL BIT MAP

The directions are hard coded in this design.

Pull-up and Pull-down resistors built into some '485 interface devices may



make the signal appear to be driven [if open] when in the tri-stated mode. Enabling the termination on a tri-stated line will yield approximately 2.5V on each side of the tri-stated driver.

The base design of the PMC_BiSerial_IO sets the direction of the signals to be set to output except for the signal group 12-15 which are inputs and IO0 which is also an input. The table is shown for future use when we plan to add in a read/write parallel port on the unused transmission lines.

<u>CONTROL</u>	<u>CORRESPONDING IO BIT(S)</u>
DIR_0..3	IO_0..3.
DIR4	IO_4..7
DIR5	IO_8..11
DIR6	IO_12..15
DIR7	IO_16..19

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others it will make sense to use the onboard terminations.

The terminations for the receive groups should be set to terminate with the user software in most cases. [term0 and term6]

<u>CONTROL</u>	<u>CORRESPONDING IO BIT(S)</u>
TERM_0..3	IO_0..3.
TERM4	IO_4..7
TERM5	IO_8..11
TERM6	IO_12..15
TERM7	IO_16..19

Fifo_tx1-3

[\$2C,30,34 Internal FIFOs read/write]

The 4 x 32 internal FIFO associated with each transmit channel 1-3 are accessed through these ports. The ports act like a partially implemented FIFO. Reading from the port will access whatever data is stored in the last position. Reading will not cause the data to progress through the FIFO. Writing will insert new data into the first register and move any data currently within the "FIFO" down one position. To read-back write four data words, read the first, then write a dummy word and read the second...repeat for next 2 positions.



bis_switch

[\$44 BiSerial Switch Read Port read only]

CONTROL REGISTER 1	
DATA BIT	DESCRIPTION
5	UB5
4	UB4
3	UB3
2	UB2
1	UB1
0	UB0

FIGURE 12

PMC-BISERIAL-PS1 SWITCH READ BIT MAP

The Switch Read Port has the user bits. The user bits are connected to 6 switch positions. The switches allow custom configurations to be defined by the user and for the software to “know” how to configure the read/write capabilities of each IO line. Please note that the lower 6 bits of the switch are implemented [8 positions on switch]. The silk-screen is marked with the ‘0’ and ‘1’ definitions. * * * unimplemented in this version * * *



Interrupts

PMC-BiSerial interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with a PMC-BiSerial interrupt the software must read the status register(s) to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly.

The PMC-BiSerial state machines generate an interrupt request when a transmission is complete and the INTEN bits in the control registers are set. The transmission is considered complete when the data has been transmitted. The interrupt is mapped to INTA on the PMC connector. INTA may be mapped to a different interrupt in your system. For example in our NT systems it is mapped to interrupt B. The source of the interrupt is obtained by reading BIS_STAT0. The status remains valid until the status register is read. The interrupt status is auto-cleared when the status register is accessed.

The interrupt level seen by the CPU is determined by the rest of the system. The master interrupt can be disabled or enabled through the bis_base register. The individual enables for TX0-3 are controllable through bis_tx.

The individual enables operate before the interrupt holding latches, which store the request for the CPU. Once the interrupt request is set, the way to clear the request is to reset the board, access bis_intc, or disable the interrupt. Toggling the interrupt enable low will clear the interrupt. The interrupt enable can be set back to enabled immediately. TX_INT_EN0-3 enables and clears the corresponding TX0-3 interrupt. The master enable is a mask and can be used to disable the interrupt from reaching the CPU, but still leaves the internal interrupt request hardware active which is useful for polled operation.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled and the TX, and programmable level interrupts enabled as needed. When bis_stat0 shows an interrupt pending the appropriate FIFO action can take place and the enable toggled to remove the interrupt request. One extra read of the bis_stat0 to make sure that the interrupt request is cleared before starting the next transfer. The first read of bis_stat0 register does clear the interrupt status. The source of the status is still pending [interrupt request] after the status read and before the enable toggle or bis_intc



operation which removes the source of the status. The status can become set again before the SW has a chance to clear the source. It is necessary to do one extra read for clearing purposes.

If operating with TX interrupts enabled and random timing, it is recommended that the individual enables be used to clear the interrupt source. It is possible that one interrupt is closely followed by another leading to the second being cleared by the response to the first before the status bit captures the event leading to a lost interrupt request. By using the individual interrupt enables to clear the interrupt, the issue is avoided because the software is only clearing the interrupt that triggered the interrupt cycle. If a second interrupt comes as described in the pathological case then it will remain after the clearing operation. The second status read may capture the event or not depending on the timing. If the second interrupt is captured by the status register then the software can either recognize the second event or choose to ignore it. If recognized the software can save an interrupt cycle by immediately processing the new information. If the information was ignored then a new interrupt request will be created. The host can treat the second interrupt as a new event.

Power on initialization will provide a cleared interrupt request and interrupts disabled.

Test

External Loop-Back is not possible with the -PS1 version because the receiver channels were removed. The transmitted data can be observed on the HDEterm68 header pins with an oscilloscope or logic analyzer. The internal FIFOs can be read-back.

The Engineering kit has reference software which includes the transmit scope test and internal FIFO tests plus Schematics, HDEterm68, cable.

Channel 0

Data+	7	Data-	41
Clk+	9	Clk-	43
Strobe+	11	Strobe-	45

Channel 1

Data+	14	Data-	48
-------	----	-------	----

Channel 2

Data+	16	Data-	50
-------	----	-------	----

Channel 3

Data+	17	Data-	51
-------	----	-------	----



PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BiSerial-PS1. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V[unused]	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 13

PMC-BISERIAL-PS1 PN1 INTERFACE



PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BiSerial-PS1. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V[unused]		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 14

PMC-BISERIAL-PS1 PN2 INTERFACE



BiSerial Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-BiSerial. Also, see the User Manual for your carrier board for more information. GND* is a plane which is tied to GND through a 1206 0% resistor. AC or open are options – contact Dynamic Engineering.

IO_0p [ref clk+]	IO_0m [ref clk-]	1	35
IO_1p	IO_1m	2	36
GND*	GND*	3	37
IO_2p	IO_2m	4	38
GND*	GND*	5	39
IO_3p	IO_3m	6	40
IO_4p [TX_DATA0+]	IO_4m [TX_DATA0-]	7	41
GND*	GND*	8	42
IO_5p [TX_CLK+]	IO_5m [TX_CLK-]	9	43
GND*	GND*	10	44
IO_6p [TX_STB+]	IO_6m [TX_STB-]	11	45
IO_7p	IO_7m	12	46
GND*	GND*	13	47
IO_8p [TX_DATA1+]	IO_8m [TX_DATA1-]	14	48
GND*	GND*	15	49
IO_9p [TX_DATA2+]	IO_9m [TX_DATA2-]	16	50
IO_10p [TX_DATA3+]	IO_10m [TX_DATA3-]	17	51
GND*	GND*	18	52
IO_11p	IO_11m	19	53
GND*	GND*	20	54
IO_12p [input0+]	IO_12m [input0-]	21	55
IO_13p [input1+]	IO_13m [input1-]	22	56
GND*	GND*	23	57
IO_14p [input2+]	IO_14m [input2-]	24	58
GND*	GND*	25	59
IO_15p	IO_15m	26	60
GND*	GND*	27	61
IO_16p	IO_16m	28	62
GND*	GND*	29	63
IO_17p	IO_17m	30	64
GND*	GND*	31	65
IO_18p	IO_18m	32	66
GND*	GND*	33	67
IO_19p	IO_19m	34	68

FIGURE 15

PMC-BISERIAL-PS1 FRONT PANEL INTERFACE



PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC-BiSerial Module routed to Pn4. Also, see the User Manual for your carrier board for more information.

IO_0p	REFCLK+	IO_0m	REFCLK-	1	2
IO_1p		IO_1m		3	4
IO_2p		IO_2m		5	6
IO_3p		IO_3m		8	9
IO_4p	TX_DATA0p	IO_4m	TX_DATA0m	9	10
IO_5p	TX_CLKp	IO_5m	TX_CLKm	11	12
IO_6p	TX_STBp	IO_6m	TX_STBm	13	14
IO_7p		IO_7m		15	16
IO_8p	TX_DATA1p	IO_8m	TX_DATA1m	17	18
IO_9p	TX_DATA2p	IO_9m	TX_DATA2m	19	20
IO_10p	TX_DATA3p	IO_10m	TX_DATA3m	21	22
IO_11p		IO_11m		23	24
IO_12p	input0p	IO_12m	input0m	25	26
IO_13p	input1p	IO_13m	input1m	27	28
IO_14p	input2p	IO_14m	input2m	29	30
IO_15p		IO_15m		31	32
IO_16p		IO_16m		33	34
IO_17p		IO_17m		35	36
IO_18p		IO_18m		37	38
IO_19p		IO_19m		39	40
				41	42
				43	44
				45	46
				47	48
				49	50
				51	52
				53	54
				55	56
				57	58
				59	60
				61	62
				63	64

FIGURE 16

PMC-BISERIAL-PS1 PN4 INTERFACE



Applications Guide

Interfacing

The pinout tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC-BiSerial when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. PMC-BISERIAL does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the BiSerial pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68 screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68

[<http://www.dyneng.com/HDEterm68.html>]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages.



Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BiSerial is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BISERIAL design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.



Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.



Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is \$100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
support@dyneng.com



Specifications

Host Interface:	PCI Mezzanine Card
Serial Interface:	RS-485 TX_Data0, TX_CLK, TX_STB, TX_Data1, TX_Data2, TX_Data3
TX CLK rates generated:	5 MHz. Other rates available with special oscillator installation
Software Interface:	Control Registers, Status Ports, FIFO
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses
Interrupt:	Tx interrupt at end of transmission Programmable Almost Empty
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/°C for uniform heat across IP
Power:	Max. TBD mA @ 5V



Order Information

PMC-BISERIAL-IO	PMC Module with 4 Tx channels, 5 MHz data rate -PS1 protocol support, RS-485 drivers and receivers 32 bit data interface
Eng Kit-PMC-BISERIAL-PS1	HDEterm68 - 68 position screw terminal adapter HDEcabl68 - 68 IO twisted pair cable Technical Documentation, 1. PMC-BISERIAL Schematic 2. PMC-BISERIAL Reference test software Data sheet reprints are available from the manufacturer's web site reference software.

Note: *The Engineering Kit is strongly recommended for first time PMC-BISERIAL buys.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.

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