

DYNAMIC ENGINEERING

150 Dubois St. Suite B/C, Santa Cruz, CA 95060 Ph: 831-457-8891 sales@dyneng.com Est. 1988

Statement of Volatility PN: PMC-Parallel-485

Manufacturer Part Number: PMC-Parallel-485, includes all types (-RIO, etc.) Manufacturer Part Description: PMC with FPGARS-485 or LVDS transceivers FPGA Type: Xilinx Spartan II– typically "150" – SRAM configuration type.

Memory Type: FLASH, SRAM

Memory Size: varies with installed FPGA

Volatility: SRAM and FIFO memories cleared by power cycle. FLASH is retained through power cycle. FLASH is not accessible by user for writing or read-back. FLASH is used to

reload FPGA at power-on.

User Accessible: SRAM within FPGA is configured into registers etc. FPGA features are R/W [in many cases] to user software. SRAM contents are lost at power down and re-written with base design from FLASH upon power-on.

Clearing Procedure: Power cycle or re-write data stored contents per approved procedure.

Notes or Warnings: None