



DYNAMIC ENGINEERING

150 Dubois St. Suite C, Santa Cruz, CA 95060

Ph: 831-457-8891 / Fax: 831-457-4793

sales@dyneng.com www.dyneng.com

Est. 1988

Statement of Volatility

PN: IP-OptoISO-16

Manufacturer Part Number: IP-OptoISO-16, includes all options (-ROHS etc.)

Manufacturer Part Description: IndustryPack Module with 16 Optical Isolators

Memory Type: FPGA and FLASH

Memory Size: FPGA Xilinx Spartan II: Internal registers for configuration of Optoisolators.

FLASH : Memory to provide power on configuration to FPGA. Not user accessible.

Volatility: FLASH is non-volatile. User Registers are volatile.

User Accessible: FIFO within FPGA if implemented are not user accessible in the traditional sense as the data is flowing through these memories without user control. Standard model does not implement at this time. Registers are tied to controls for FET's etc. User accessible, but only control not used for user data.

Clearing Procedure: Use and Power cycle for FIFO/Register memory. To clear the FLASH a standard 3 pass write cycle would be required.

Notes or Warnings: None