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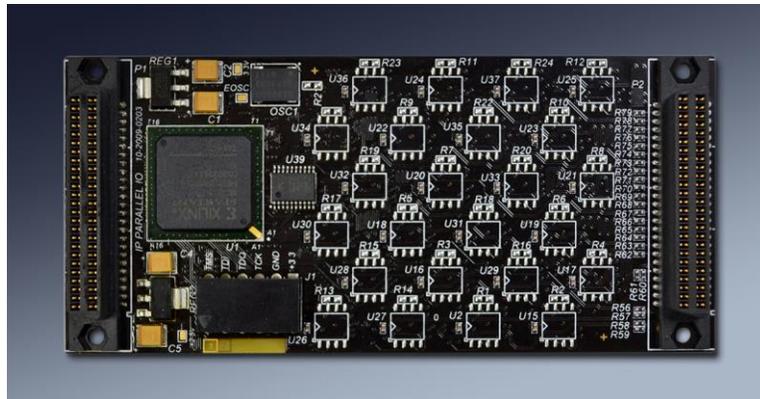
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Est. 1988

User Manual IP-Parallel-IO Digital Parallel Interface IP Module



| | |
|-----------------|------|
| 48 TTL / 0 485 | -TTL |
| 40 TTL / 4 485 | -1 |
| 32 TTL / 8 485 | -2 |
| 24 TTL / 12 485 | -3 |
| 16 TTL / 16 485 | -4 |
| 8 TTL / 20 485 | -5 |
| 0 TTL / 24 485 | -485 |

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Corresponding Hardware: Revision 03

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IP-Parallel-IO
Digital Parallel Interface
IP Module
Dynamic Engineering

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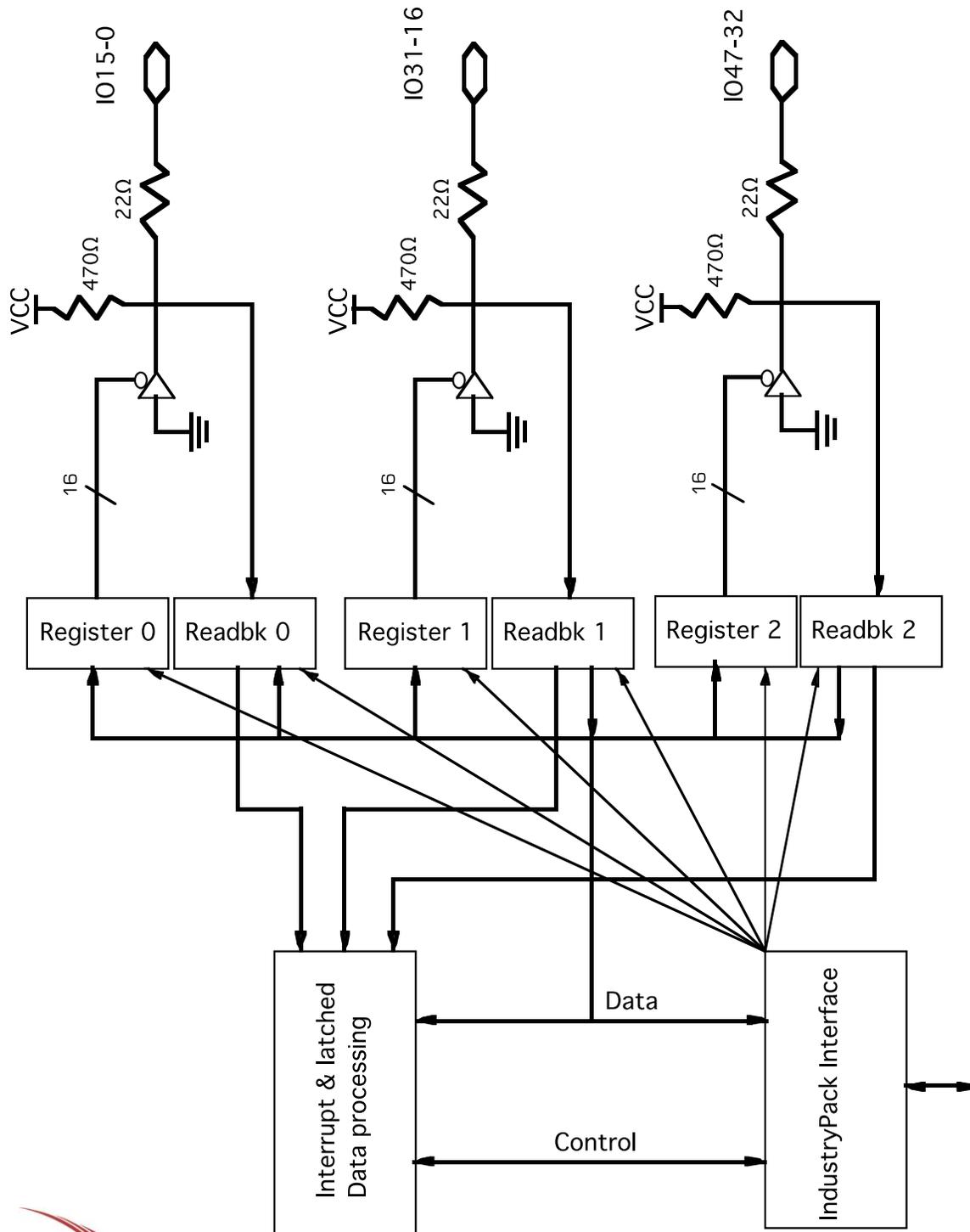


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Product Description and Operation



IP-Parallel-IO is part of the IP Module family of modular I/O components. IP-Parallel-IO is capable of providing multiple protocols. The TTL version provides 48 uncommitted IO. Each channel can be programmed to be input, output and interrupter. The 485 version has 24 differential pairs. TTL and Differential pairs can be mixed to have any combination of TTL and Differential IO. Please refer to the ordering table to see the standard IO options.

Each TTL bit has a register bit associated with it. When the register bit is set to '0' that channel turns on the open-drain driver and puts a '0' on the line. When the register bit is set to '1' then the open drain driver is turned off and the pull-up will create a high level on the line unless some other system element is driving the line low. The register is read-write and will always return the value written to it. There are 48 IO lines. Three 16 bit wide registers are dedicated to the Control [CNTL] bus.

The CNTL bus is supported by a synchronization control bit in the base register. The control registers are double buffered with the second register level connected to the IO. The synchronization bit enables the second level registers to update or hold. Clearing the enable before updating and re-enabling after the primary registers have new values will allow the 48 IO to be synchronously updated through the second level of registers. If left enabled the CNTL will be updated one clock after the register is updated. If disabled, then the last enabled control setting is held. The reset default is 'FFFFFFFFFFFF' to turn the drivers off in TTL mode.

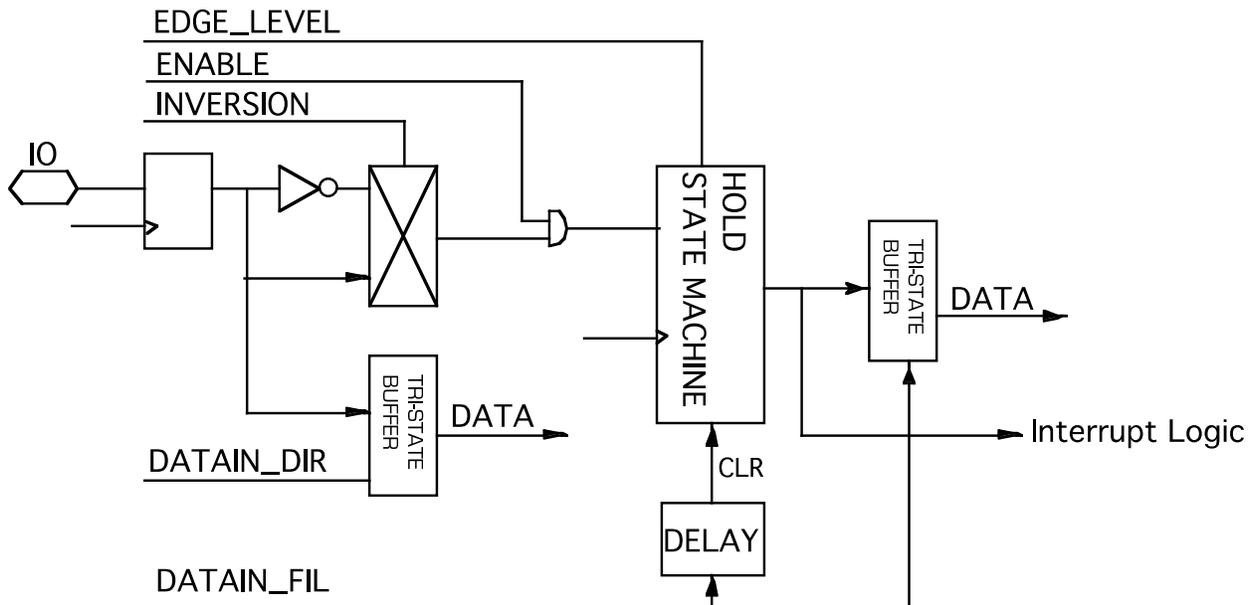
Each IO line is also brought into the FPGA [Xilinx Spartan II]. The IO lines are available as a direct read or after filtering. The data read from the IO will match the register bits if there are no other drivers in the system. The IO bits may not match if an external device is attached.

Each channel has an enable, sense, and edge or level bit associated with it. The enable will block or enable a particular channel from being received into the filtered logic. The sense will either keep the current version or invert the data received. The edge or level control will make the hold circuit wait for an edge from 0 > 1 or react to a level. The hold circuit captures data and holds it until read. The data is registered at the chip edge, and again after the enable and inversion circuitry. Each bit has a separate hold circuit. If a signal is detected high then the signal is held until the data is read. With the inversion capability each channel can be programmed to "be high" or to transition to a high condition when the channel has something of interest.

The registers are referenced to the IP clock and operate at 8 or 32 MHz depending on the slot configuration. Each group of 16 channels has a separate read clear signal. The channels can be read in any order and not loose data. The circuit will capture pulses



down to 2 reference clocks wide. 62.5 nS or 250 nS with the standard IP reference clock.



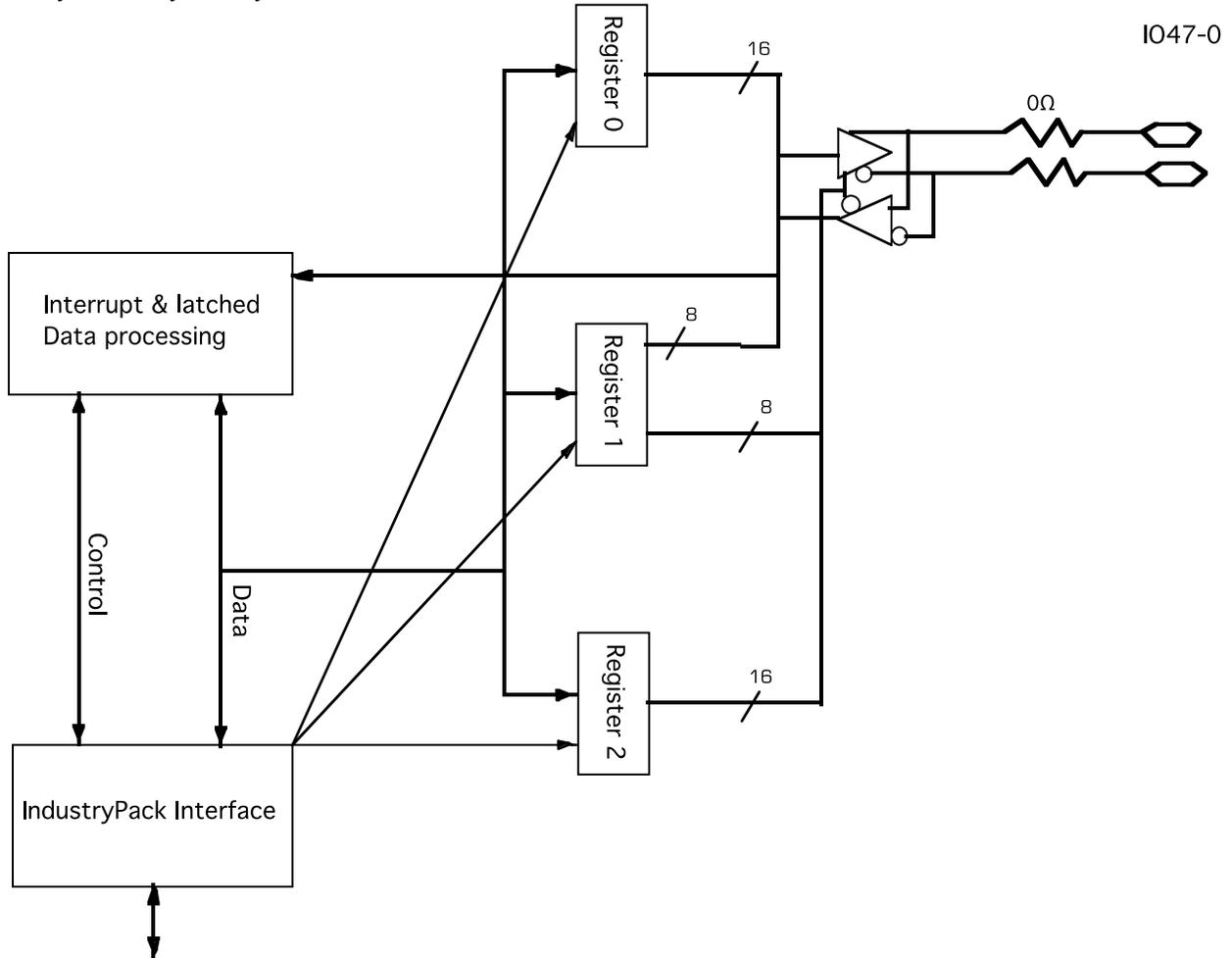
The active high signals are combined to create an interrupt request based on the captured and held data. If the master interrupt enable is “enabled” the interrupt is passed to the system. The interrupt is cleared by reading the data or disabling the master enable. The user can program each channel to use the edge or level condition. The edge is particularly useful for long duration signal where repeated interrupts are not desired. The alternate approach is to flip the sense bit and create an interrupt when the signal has switched to the opposite polarity.

Instruction order is important. Once the interrupt is detected the sense needs to be switched before the interrupt is re-enabled or a second interrupt is likely to be generated. It is recommended to read from the filtered data path after the processing parameters are changed to clear any interrupts that are created by the changing filter parameters.

With each IO line having all three controls plus independent direction a lot of interrupt possibilities exist.

The TTL IO can be substituted with 485 transceivers. Each transceiver uses 2 IO lines for a maximum of 24. The driver and pull-up combination used creates a minimum group of 8 TTL IO or 4 Differential IO to swap. There are 7 standard versions of the board. The TTL version with all TTL IO, the 485 version with all 485 IO and mixed versions with 8, 16, 24, 32, and 40 of the IO dedicated to TTL and the rest with 485 IO.

Each FLASH version is populated with a different IDPROM to make card identification easy within your system.



In the versions with 485 transceivers the control bits have an alternate definition. The bits are paired; one the direction control and one the data bit. In the TTL version, all of the bits are data bits. Please refer to the diagram of the -485 version.

When the 485 transceivers are added in place of the TTL drivers, new control definitions occur. For ease of use the control registers are re-mapped between the different versions to group the direction bits and the data bits together at the upper end of the control words [cntl0-2]. The space is divided in half with the upper half used for the control and the lower half for data. In the case with only 485 transceivers the lower 24 bits are data and the upper 24 control. In the -1 case the upper 8 bits are used for 485 with the 40-43 used for data and 44-47 for control. The bits are remapped to the hardware locations within the FPGA. By re-mapping, the data can be written in a

natural order if used as a bus. A 0x04 is a 0x04. Without re-mapping, the data bits would be separated by the control bits, and broken into two sections. The groups of 8 are really implemented as two groups of 4. IO47-44 and IO23-20 represent the first group. The re-mapping will put the control and data on cntl40-47. IO47, 45, 23, 21 are the physical control bits. A result of re-mapping the data is normally ordered and more conveniently located. Please refer to the Bit Mapping Table in the programming section.

In addition to the IO version, other custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there, we can redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please contact Dynamic Engineering with your custom application. Several of the IO bits are implemented on the long line clock pins of the FPGA. External clock references can be designed in as a custom option. There is a user oscillator position to support custom state machines and IO requirements. The DMA controls, second interrupt level, and memory space controls are routed to the FPGA to allow for future upgrades.

IP-PARALLEL-IO supports both 8 and 32 Mhz. IP Bus operation. All configuration registers support read and write operations for maximum software convenience. Word operations are supported (please refer to the memory map). The ID, IO, and INT spaces are utilized by the IP-Parallel-IO design.

IP-PARALLEL-IO conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. The PCI3IP or PCIe3IP cards make a convenient development platform in many cases.

http://www.dyneng.com/pci_3_ip.html, <http://www.dyneng.com/PCIe3IP.html>

Interrupts are supported by IP-PARALLEL-IO. The interrupt occurs when a programmed transition occurs. The interrupts are individually maskable – each IO channel has a separate mask. The vector is user programmable by a read/write register. The interrupt occurs on IntReq0. The vector can be read in the IO space or automatically with the INT space.

Frequently it is necessary to correlate the time and the event. The IP-Parallel design supports an enhanced MC68230 capability with two - 32 bit counter - timers. The counter-timers are easy to use with a minimum of registers to access and complete independence. The IP clock is used as a reference; both 8 and 32 MHz can be used.

Counter/Timer A features a 32 bit down-counter with a pre-load register. The counter



output is tested against a "zero" value. When zero the counter is re-loaded with the pre-load value to create a cycle. At each zero detection an interrupt can be generated. At each zero detection a waveform can be transitioned. The waveform can be enabled onto the upper data bit.

For the –TTL model this will be a TTL signal, for all other models the MSB will be a differential pair. For the non TTL models [-1 ⇔ -5, -485] the corresponding direction control bit for the 485 buffer will also need to be set to drive the waveform onto the IO lines.

Counter / Timer B has a 32 bit up counter which can be cleared by the software. The counter output is masked with a user programmable value to select a particular counter bit or bits to use for interrupt creation. The counter output is also available to read via software and can serve as a real-time clock

Address Map

| Function | Offset | Width | Type |
|-----------------|-----------------------|-------|------------|
| cntl0 | EQU \$00 | word | read/write |
| cntl1 | EQU \$02 | word | read/write |
| cntl2 | EQU \$04 | word | read/write |
| Base_cntl | EQU \$06 | word | read/write |
| Int En0 | EQU \$08 | word | read/write |
| Int En1 | EQU \$0A | word | read/write |
| Int En2 | EQU \$0C | word | read/write |
| vector | EQU \$0E | word | read/write |
| Int EdgLvl0 | EQU \$10 | word | read/write |
| Int EdgLvl1 | EQU \$12 | word | read/write |
| Int EdgLvl2 | EQU \$14 | word | read/write |
| | | | |
| Int Pol0 | EQU \$18 | word | read/write |
| Int Pol1 | EQU \$1A | word | read/write |
| Int Pol2 | EQU \$1C | word | read/write |
| status | EQU \$1E | word | read/write |
| dat_in_fil0 | EQU \$20 | word | read |
| dat_in_fil1 | EQU \$22 | word | read |
| dat_in_fil2 | EQU \$24 | word | read |
| | | | |
| dat_in_dir0 | EQU \$28 | word | read |
| dat_in_dir1 | EQU \$2A | word | read |
| dat_in_dir2 | EQU \$2C | word | read |
| | | | |
| pre_load_l | EQU \$2E | word | read/write |
| pre_load_u | EQU \$30 | word | read/write |
| mask_l | EQU \$32 | word | read/write |
| mask_u | EQU \$34 | word | read/write |
| rdbk_l | EQU \$36 | word | read |
| rdbk_u | EQU \$38 | word | read |
| | | | |
| Parallel_IDPROM | byte on word boundary | | read |

FIGURE 1

IP-PARALLEL-IO INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within IP-PARALLEL-IO. The addresses are all offsets from a base address. The carrier board that the IP is installed into provides the base address.

Programming

Programming IP-PARALLEL-IO requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Carrier board.

In order to receive data the software is only required to read from the "Direct" port. Alternatively the filtered data path can be programmed with the enable, Level and edge and then the Filtered data used. If desired, the interrupt can be enabled and the interrupt vector written to the vector register.

A typical sequence would be to first write to the vector register with the desired interrupt vector. Please note that many carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the mask should be set. The Level and Edge conditions programmed, then the enables set to receive data. The incoming data can be pulsed. The hardware will hold any pulse or level detected until the data is read by software.

Data is written to the Control [cntl] registers. Any active low bits are used to enable the open drain drivers. The drivers have 24 mA sink capability and overcome the pull-up [10 mA] to create a '0' on the bus. A '1' in a bit position turns off the driver leaving the pull-up to set the level to a '1'. Other hardware in the system can also pull the signal line to '0'. If enabled, the lines controlled by the outputs can cause interrupts back to the host. Usually these will be disabled to prevent self-interrupting.

When 485 transceivers are installed the driver section creates a differential signal pair. The pull-up resistors are not installed. A software written '1' will result in the + side driven high and the - side driven to ground. A software written '0' will result in the + side driven to ground and the minus side driven high.

A 32 bit write/read with some carriers will result in two 16 bit accesses to the hardware with automatic incrementing addresses. The 32 bit access is quite a bit faster than a software loop. Dynamic Engineering IP Carriers support 32 bit to 16 bit mapping automatically. The lower 32 bits of the output, "data in filtered", and "data in direct" are on long word boundaries to utilize this feature if available.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.



Register Definition

CNTL0-TTL:

\$00 Parallel Control Register Port read/write

| CONTROL REGISTER 0 | |
|--------------------|------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 15-0 output data control bits |

FIGURE 2-TTL

IP-PARALLEL-TTL CONTROL REGISTER 0 BIT MAP

CNTL1-TTL

\$02 Parallel Control Register Port read/write

| CONTROL REGISTER 1 | |
|--------------------|-------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 31-16 output data control bits |

FIGURE 3-TTL

IP-PARALLEL-TTL CONTROL REGISTER 1 BIT MAP

CNTL2-TTL

\$04 Parallel Control Register Port read/write

| CONTROL REGISTER 2 | |
|--------------------|-------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 47-32 output data control bits |

FIGURE 4-TTL

IP-PARALLEL-TTL CONTROL REGISTER 2 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF', off state for TTL mode and default to inputs in 485 mode.
2. In TTL mode each CNTL bit directly corresponds to an IO bit.
3. In mixed and 485 modes the cntl bits are re-mapped to push the 485 definitions to the upper bits, and to separate data and direction.

CNTL0-1

\$00 Parallel Control Register Port read/write

| CONTROL REGISTER 0 | |
|--------------------|------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 15-0 output data control bits |

FIGURE 2-1

IP-PARALLEL-1 CONTROL REGISTER 0 BIT MAP

CNTL1-1

\$02 Parallel Control Register Port read/write

| CONTROL REGISTER 1 | |
|--------------------|-------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 31-16 output data control bits |

FIGURE 3-1

IP-PARALLEL-1 CONTROL REGISTER 1 BIT MAP

CNTL2-1

\$04 Parallel Control Register Port read/write

| CONTROL REGISTER 2 | |
|--------------------|-------------------------------------|
| DATA BIT | DESCRIPTION |
| 7-0 | cntl 39-32 output data control bits |
| 11-8 | 485 data [IO43-40] |
| 15-12 | 485 direction 1 = TX |

FIGURE 4-1

IP-PARALLEL-1 CONTROL REGISTER 2 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF', off state for TTL mode and default to inputs in 485 mode.
2. In TTL mode each CNTL bit directly corresponds to an IO bit.
3. In mixed and 485 modes the cntl bits are re-mapped to push the 485 definitions to the upper bits, and to separate data and direction.

CNTL0-2

\$00 Parallel Control Register Port read/write

| CONTROL REGISTER 0 | |
|--------------------|------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 15-0 output data control bits |

FIGURE 2-2

IP-PARALLEL-2 CONTROL REGISTER 0 BIT MAP

CNTL1-2

\$02 Parallel Control Register Port read/write

| CONTROL REGISTER 1 | |
|--------------------|-------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 31-16 output data control bits |

FIGURE 3-2

IP-PARALLEL-2 CONTROL REGISTER 1 BIT MAP

CNTL2-2

\$04 Parallel Control Register Port read/write

| CONTROL REGISTER 2 | |
|--------------------|----------------------|
| DATA BIT | DESCRIPTION |
| 7-0 | 485 data [IO39-32] |
| 15-8 | 485 direction 1 = TX |

FIGURE 4-2

IP-PARALLEL-2 CONTROL REGISTER 2 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF', off state for TTL mode and default to inputs in 485 mode.
2. In TTL mode each CNTL bit directly corresponds to an IO bit.
3. In mixed and 485 modes the cntl bits are re-mapped to push the 485 definitions to the upper bits, and to separate data and direction.

CNTL0-3

\$00 Parallel Control Register Port read/write

| CONTROL REGISTER 0 | |
|--------------------|------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 15-0 output data control bits |

FIGURE 2-3

IP-PARALLEL-3 CONTROL REGISTER 0 BIT MAP

CNTL1-3

\$02 Parallel Control Register Port read/write

| CONTROL REGISTER 1 | |
|--------------------|-------------------------------------|
| DATA BIT | DESCRIPTION |
| 7-0 | cntl 23-16 output data control bits |
| 15-8 | 485 data [IO31-24] |

FIGURE 3-3

IP-PARALLEL-3 CONTROL REGISTER 1 BIT MAP

CNTL2-3

\$04 Parallel Control Register Port read/write

| CONTROL REGISTER 2 | |
|--------------------|--------------------------------|
| DATA BIT | DESCRIPTION |
| 3-0 | 485 data [IO35-32] |
| 15-4 | 485 direction 1 = TX [IO35-24] |

FIGURE 4-3

IP-PARALLEL-3 CONTROL REGISTER 2 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF', off state for TTL mode and default to inputs in 485 mode.
2. In TTL mode each CNTL bit directly corresponds to an IO bit.
3. In mixed and 485 modes the cntl bits are re-mapped to push the 485 definitions to the upper bits, and to separate data and direction.

CNTL0-4

\$00 Parallel Control Register Port read/write

| CONTROL REGISTER 0 | |
|--------------------|------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | cntl 15-0 output data control bits |

FIGURE 2-4

IP-PARALLEL-4 CONTROL REGISTER 0 BIT MAP

CNTL1-4

\$02 Parallel Control Register Port read/write

| CONTROL REGISTER 1 | |
|--------------------|--------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | 485 data [IO31-16] |

FIGURE 3-4

IP-PARALLEL-4 CONTROL REGISTER 1 BIT MAP

CNTL2-4

\$04 Parallel Control Register Port read/write

| CONTROL REGISTER 2 | |
|--------------------|--------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | 485 direction 1 = TX [IO31-16] |

FIGURE 4-4

IP-PARALLEL-4 CONTROL REGISTER 2 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF', off state for TTL mode and default to inputs in 485 mode.
2. In TTL mode each CNTL bit directly corresponds to an IO bit.
3. In mixed and 485 modes the cntl bits are re-mapped to push the 485 definitions to the upper bits, and to separate data and direction.

CNTL0-5

\$00 Parallel Control Register Port read/write

| CONTROL REGISTER 0 | |
|--------------------|-----------------------------------|
| DATA BIT | DESCRIPTION |
| 7-0 | cntl 7-0 output data control bits |
| 15-8 | 485 data [IO15-8] |

FIGURE 2-5

IP-PARALLEL-5 CONTROL REGISTER 0 BIT MAP

CNTL1-5

\$02 Parallel Control Register Port read/write

| CONTROL REGISTER 1 | |
|--------------------|-------------------------------|
| DATA BIT | DESCRIPTION |
| 11-0 | 485 data [IO27-16] |
| 15-12 | 485 direction 1 = TX [IO11-8] |

FIGURE 3-5

IP-PARALLEL-5 CONTROL REGISTER 1 BIT MAP

CNTL2-5

\$04 Parallel Control Register Port read/write

| CONTROL REGISTER 2 | |
|--------------------|--------------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | 485 direction 1 = TX [IO27-12] |

FIGURE 4-5

IP-PARALLEL-5 CONTROL REGISTER 2 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF', off state for TTL mode and default to inputs in 485 mode.
2. In TTL mode each CNTL bit directly corresponds to an IO bit.
3. In mixed and 485 modes the cntl bits are re-mapped to push the 485 definitions to the upper bits, and to separate data and direction.

CNTL0-485

\$00 Parallel Control Register Port read/write

| CONTROL REGISTER 0 | |
|--------------------|-------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | 485 data [IO15-0] |

FIGURE 2-485

IP-PARALLEL-485 CONTROL REGISTER 0 BIT MAP

CNTL1-485

\$02 Parallel Control Register Port read/write

| CONTROL REGISTER 1 | |
|--------------------|-----------------------|
| DATA BIT | DESCRIPTION |
| 7-0 | 485 data [IO23-16] |
| 15-8 | 485 Direction [IO7-0] |

FIGURE 3-485

IP-PARALLEL-485 CONTROL REGISTER 1 BIT MAP

CNTL2-485

\$04 Parallel Control Register Port read/write

| CONTROL REGISTER 2 | |
|--------------------|------------------------|
| DATA BIT | DESCRIPTION |
| 15-0 | 485 direction [IO23-8] |

FIGURE 4-485

IP-PARALLEL-485 CONTROL REGISTER 2 BIT MAP

1. All bits are active low and are reset on power-up. Default to 'FFFF', off state for TTL mode and default to inputs in 485 mode.
2. In TTL mode each CNTL bit directly corresponds to an IO bit.
3. In mixed and 485 modes the cntl bits are re-mapped to push the 485 definitions to the upper bits, and to separate data and direction.

Bit Mapping Tables

“-TTL” (48 TTL lines)

| <u>IO</u> | <u>CNTL (#/Definition)</u> |
|-----------|----------------------------|
| 47-0 | 47-0/TTL level IO [IO47-0] |

“-1” (40 TTL and 4 – ‘485)

| <u>IO</u> | <u>CNTL (#/Definition)</u> |
|-------------|--|
| 47-44,23-20 | 47-44/485 direction control 43-40/485 data bits [IO43-40] |
| 43-24,19-0 | 39-0/TTL Level IO [IO39-0] |

“-2” (32 TTL and 8 – ‘485)

| <u>IO</u> | <u>CNTL (#/Definition)</u> |
|-------------|--|
| 47-40,23-16 | 47-40/485 direction control 39-32/485 data bits [IO39-32] |
| 39-24,15-0 | 31-0/TTL Level IO [IO31-0] |

“-3” (24 TTL and 12 – ‘485)

| <u>IO</u> | <u>CNTL (#/Definition)</u> |
|-------------|--|
| 47-36,23-12 | 47-36/485 direction control 35-24/485 data bits [IO35-24] |
| 35-24,11-0 | 23-0/TTL Level IO [IO23-0] |

“-4” (16 TTL and 16 – ‘485)

| <u>IO</u> | <u>CNTL (#/Definition)</u> |
|------------|--|
| 47-32,23-8 | 47-32/485 direction control 31-16/485 data bits [IO31-16] |
| 31-24,7-0 | 15-0/TTL Level IO [IO15-0] |

“-5” (8 TTL and 20 – ‘485)

| <u>IO</u> | <u>CNTL (#/Definition)</u> |
|------------|--|
| 47-28,23-4 | 47-28/485 direction control 27-8/485 data bits [IO27-8] |
| 27-24,3-0 | 7-0/TTL Level IO [IO7-0] |

“-485” (24 – ‘485)

| <u>IO</u> | <u>CNTL (#/Definition)</u> |
|-----------|--|
| 47-0 | 47-24/485 direction control 23-0/485 data bits [IO23-0] |

Please note: (1) IO numbers above are re-arranged to put TTL together and 485 together. Actual IO numbers on the schematic are different. (2) differential pairs are



composed of adjacent IO pairs. For example: IO47 IO46 are a pair; when in the –1 through –485 mode. Please refer to the IO tables for complete pin assignments.

Base_CNTL

\$06 BISERIAL Control Register Port read/write

| CONTROL REGISTER BASE | |
|-----------------------|--------------------------------------|
| DATA BIT | DESCRIPTION |
| 15 | spare |
| 14 | hold timerB 0 = disabled, 1 = hold |
| 13 | clear timerB 0 = run, 1 = clear |
| 12 | interrupt enable timerB 1 = enabled |
| 11 | spare |
| 10 | square wave output 1 = output on msb |
| 9 | timerA load 0 = run , 1 = load |
| 8 | interrupt enable timerA 1 = enabled |
| 7-3 | spare |
| 2 | force interrupt 1 = force |
| 1 | master interrupt enable 1 = enabled |
| 0 | output register control 1 = enabled |

FIGURE 5 IP-PARALLEL-IO BASE CONTROL REGISTER BIT MAP

1. Output Register Control is used to control when the three Control registers values are placed onto the output registers. If synchronization is needed set to '0' until the registers are written and then enable ['1']. The output bits will then be driven to the new state at the same time. Referenced to the IP Clock. If the bit is left in the '0' state, the new control register values will not be output and the data will stay in the previous state. If the bit is left in the '1' state the control outputs will change when the registers are independently updated. *Note: Leave set to '0' until the Control Registers are initialized to your default system values to prevent contention on the lines. Enabling when uninitialized may cause IO conflicts with both ends driving etc.*

2. INT_EN is the master interrupt enable. Default is 0. If set to 1 then if one or more of the filtered input data or timer interrupt conditions is met an interrupt will be generated on level 0.

3. Force Interrupt is used to create an interrupt for test and software development purposes. Set the bit to cause an interrupt and clear the bit to remove the interrupt. The IO bits can be used for the same purpose if the filter controls are properly set. Requires INT_EN to be enabled.



4. Interrupt Enable TimerA. When enabled and the Counter/Timer A is active the counter timer will create an interrupt stream. The period of the interrupts is determined by the pre-load register. The interrupt is generated when the Counter/Timer A counts down to “0”. Requires INT_EN to be enabled.

5. Counter/Timer A load when ‘1’ loads the value in the preload register into the down counter. When ‘0’ the counter decrements until the terminal count of “0” is reached at which point the counter re-loads the pre-load value and repeats the cycle. The load bit is not needed because the counter will eventually roll over and reload anyway. If a large count was previously loaded or if the software wants to have a consistent period from a known point in time then the load bit should be used.

6. WaveOut when enabled selects the waveform generated by Counter/Timer A to output on the MSBit instead of the data bit for that position. 1 = waveform, 0 = databit. The waveform is a square wave which is switched at each zero crossing – has 2x period of the interrupts generated by Counter/Timer A.

7. Interrupt Enable Counter/Timer B when ‘1’ creates an interrupt stream based on the second counter timer. Counter/Timer B is a 32 bit up counter. The counter output is masked with the value in the mask register to pick off the period you desire for the interrupt stream. For example: with the IP clock set to 8 Mhz and the mask set to a 0x00000040 the 7th bit would be selected for a divide by $64 \times 2 \times 125 = 16 \mu\text{s}$ period. Requires INT_EN to be enabled to cause an interrupt.

8. Clear Counter/Timer B when ‘1’ forces the second counter timer to 0. This function is useful to restart the “real time clock” to a known value at a known time.

9. Hold Timer when ‘1’ will stop the Counter/Timer B from updating the read-back register. Counter/Timer B will continue to run. The register will be stable allowing the two reads of the register data to happen without the stored count changing. “0” = update the counter read-back register.



INTerrupt Enable

Int_en0 \$08 Parallel Control Register Port read/write

| DATA BIT | Interrupt Enable DESCRIPTION |
|----------|---|
| 15-0 | int_en 15-0 Interrupt Enable 1 = enabled, 0 = disabled |

FIGURE 6 IP-PARALLEL-IO INTERRUPT ENABLE 0 BIT MAP

Int_en1 \$0A Parallel Control Register Port read/write

| DATA BIT | Interrupt Enable DESCRIPTION |
|----------|--|
| 15-0 | int_en 31-16 Interrupt Enable 1 = enabled, 0 = disabled |

FIGURE 7 IP-PARALLEL-IO INTERRUPT ENABLE 1 BIT MAP

Int_en2 \$0C Parallel Control Register Port read/write

| DATA BIT | Interrupt Enable DESCRIPTION |
|----------|--|
| 15-0 | int_en 47-32 Interrupt Enable 1 = enabled, 0 = disabled |

FIGURE 8 IP-PARALLEL-IO INTERRUPT ENABLE 2 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is enabled to be a potential interrupter and to be captured by the hold circuit. The enable is applied after the inversion control. [In 485 mode the bits corresponding to the direction control should be set to '0'](#).

INTerrupt Edge_Lvl

Edg_Lvl 0 \$10 Parallel Control Register Port read/write

| DATA BIT | EDGE_LVL | DESCRIPTION |
|-----------------|-----------------|--------------------------------------|
| 15-0 | | Edge_Lvl 15-0 1 = edge, 0 = level |

FIGURE 9 IP-PARALLEL-IO INTERRUPT EDG_LVL 0 BIT MAP

Edg_Lvl 1 \$12 Parallel Control Register Port read/write

| DATA BIT | EDGE_LVL | DESCRIPTION |
|-----------------|-----------------|---------------------------------------|
| 15-0 | | Edge_Lvl 31-16 1 = edge, 0 = level |

FIGURE 10 IP-PARALLEL-IO INTERRUPT EDG_LVL 1 BIT MAP

Edg_Lvl 2 \$14 Parallel Control Register Port read/write

| DATA BIT | EDGE_LVL | DESCRIPTION |
|-----------------|-----------------|---------------------------------------|
| 15-0 | | Edge_Lvl 47-32 1 = edge, 0 = level |

FIGURE 11 IP-PARALLEL-IO INTERRUPT EDG_LVL 2 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is captured only if there is a transition from '0' to '1'. If set to '0' then anytime the IO line is detected to be '1' the hold circuit will be set. The hold circuit will retain the data until read by the corresponding data_in_fi(x) is accessed. The hold circuits are after the enable and inversion in the pipeline. In 485 mode the bits corresponding to the direction control should be set to '0'.

INTerrupt Polarity

Pol 0 \$18 Parallel Control Register Port read/write

| DATA BIT | Polarity | DESCRIPTION |
|----------|----------|--|
| 15-0 | | POL 15-0 1 = invert, 0 = not inverted |

FIGURE 12

IP-PARALLEL-IO INTERRUPT POL 0 BIT MAP

Pol 1 \$1A Parallel Control Register Port read/write

| DATA BIT | Polarity | DESCRIPTION |
|----------|----------|---|
| 15-0 | | POL 31-16 1 = invert, 0 = not inverted |

FIGURE 13

IP-PARALLEL-IO INTERRUPT POL 1 BIT MAP

Pol 2 \$1C Parallel Control Register Port read/write

| DATA BIT | Polarity | DESCRIPTION |
|----------|----------|---|
| 15-0 | | POL 47-32 1 = invert, 0 = not inverted |

FIGURE 14

IP-PARALLEL-IO INTERRUPT POL 2 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is inverted. If set to '0' then no inversion is applied. *In 485 mode the bits corresponding to the direction control should be set to '0'.*

Data Input Filtered

Datoin_fil0 \$20 Parallel Control Register Port read/write

| DATA BIT | Filtered Data DESCRIPTION |
|-----------------|--------------------------------------|
| 15-0 | DATAIN_FIL 15-0 |

FIGURE 15 IP-PARALLEL-IO INTERRUPT DATAIN_FIL0 BIT MAP

Datoin_fil1 \$22 Parallel Control Register Port read/write

| DATA BIT | Filtered Data DESCRIPTION |
|-----------------|--------------------------------------|
| 15-0 | DATAIN_FIL 31-16 |

FIGURE 16 IP-PARALLEL-IO INTERRUPT DATAIN_FIL1 BIT MAP

Datoin_fil2 \$24 Parallel Control Register Port read/write

| DATA BIT | Filtered Data DESCRIPTION |
|-----------------|--------------------------------------|
| 15-0 | DATAIN_FIL 47-32 |

FIGURE 17 IP-PARALLEL-IO INTERRUPT DATAIN_FIL2 BIT MAP

The data bits correspond to the IO lines after the filters have been applied. The data remains latched until the register is read. The three registers are independent for reading and clearing purposes. In 485 mode, the bits corresponding to the control are forced to '0'. Read [clear] the registers after any control change to insure that no false positives are reported

Data Input Direct

Datain_dir0 \$28 Parallel Control Register Port read/write

| DATA BIT | Direct Data DESCRIPTION |
|-----------------|--|
| 15-0 | DATAIN_DIR 15-0 |

FIGURE 18

IP-PARALLEL-IO INTERRUPT DATAIN_DIR0 BIT MAP

Datain_dir1 \$2A Parallel Control Register Port read/write

| DATA BIT | Direct Data DESCRIPTION |
|-----------------|--|
| 15-0 | DATAIN_DIR 31-16 |

FIGURE 19

IP-PARALLEL-IO INTERRUPT DATAIN_DIR1 BIT MAP

Datain_dir2 \$2C Parallel Control Register Port read/write

| DATA BIT | Direct Data DESCRIPTION |
|-----------------|--|
| 15-0 | DATAIN_DIR 47-32 |

FIGURE 20

IP-PARALLEL-IO INTERRUPT DATAIN_DIR2 BIT MAP

The data bits correspond to the IO lines without filters being applied. The data is a direct reflection of the current state of the IO lines. Metastable protection registers are in place but no hold registers. In 485 mode, the bits corresponding to the control are forced to '0'.

Pre-Load Registers

pre_load_l \$2E Parallel Control Register Port read/write

| DATA BIT | Counter Preload Data DESCRIPTION |
|----------|----------------------------------|
| 15-0 | pre-load 15-0 |

FIGURE 21

IP-PARALLEL-IO PRE-LOAD LOWER BIT MAP

Pre_load_u \$30 Parallel Control Register Port read/write

| DATA BIT | Counter Preload Data DESCRIPTION |
|----------|----------------------------------|
| 15-0 | pre_load 31-16 |

FIGURE 22

IP-PARALLEL-IO PRE-LOAD UPPER BIT MAP

The pre-load registers are combined internally to form a 32 bit pre-load value to use with Counter/Timer A. Counter/Timer A is loaded with the value in the Pre-Load registers when the counter reaches zero. The counter can also be loaded with the software command via the Base register. The counter will count from the value down to zero creating an N+1 total count. The counter will re-load the value on the next count.

The Counter Timer A has the option of creating an interrupt at each zero crossing – period N+1. The wave out option can also be enabled. The waveform is generated by switching each time the zero count is detected. A square wave is generated with a period of 2(N+1). The reference period is the IP clock, 125 nS or 31.25 nS depending on the carrier selection made.

Because of the architecture the period selected with Counter/Timer A is arbitrary. Most OS/CPU cannot handle interrupts faster than 10 uS. The counter output is registered and then checked against a count of 2 and re-registered. The count value checked is '2' to account for the double pipeline delay. The counter will be at "0" when the check reaches "2". Because of the checking scheme the minimum count needs to be larger than '2' or the hardware will miss the first "2" and not see it until the counter rolls over. At 8 MHz. The roll over time is approximately 9 minutes.



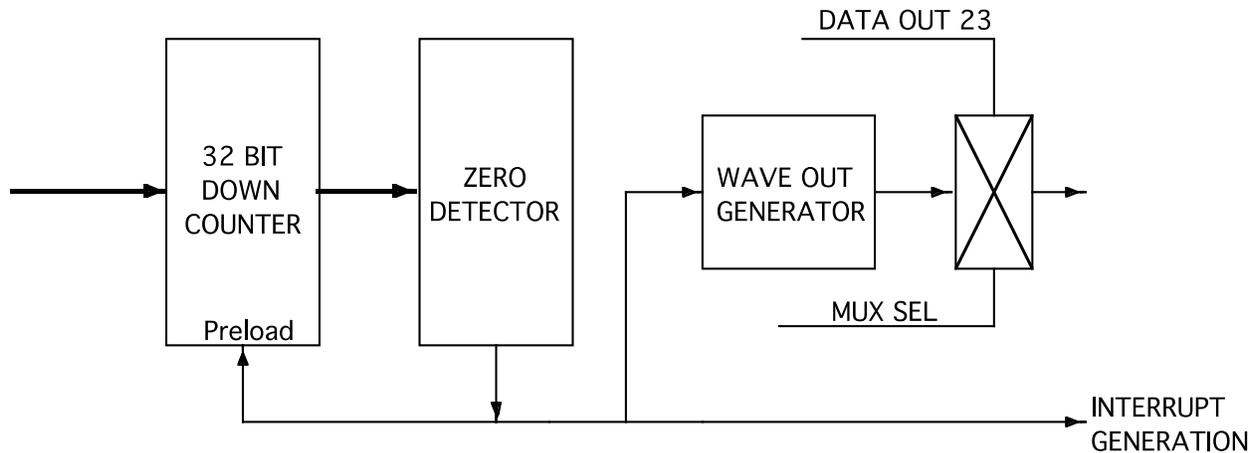


FIGURE 23

IP-PARALLEL-IO COUNTER/TIMER A

Mask Registers

mask_l \$32 Parallel Control Register Port read/write

| DATA BIT | Mask Data | DESCRIPTION |
|----------|-----------|-------------|
| 15-0 | | mask 15-0 |

FIGURE 24

IP-PARALLEL-IO MASK LOWER BIT MAP

mask_u \$34 Parallel Control Register Port read/write

| DATA BIT | Mask Data | DESCRIPTION |
|----------|-----------|-------------|
| 15-0 | | mask 31-16 |

FIGURE 25

IP-PARALLEL-IO MASK UPPER BIT MAP

The mask registers are combined internally to form a 32 bit mask value to use with Counter/Timer B. Counter/Timer B is a 32 bit up counter which can be cleared to '0'. The counter rolls over at the maximum count. Each counter bit is masked with the mask registers corresponding position. If the Mask(n) = '1' and the counter(n) is also a '1' then the output will be '1'. The output from the AND array is or'd to determine if any

of the counter bit – mask combinations are active. When a counter bit becomes active and the mask is set an interrupt is generated. The interrupt will be generated on the period of the counter selected with the mask. The counter uses the IP clock as a reference. The period selected is $2 * 2(n) * [125 \text{ or } 31.25]$. For example a 0x40 and 8 MHz reference rate would create a periodic interrupt with a period of 16 uS. [$2*64*125 \text{ nS}$]

Read-Back Registers

rdbk_l \$36 Parallel Control Register Port read/write

| DATA BIT | Count Data DESCRIPTION |
|----------|------------------------|
| 15-0 | read-back 15-0 |

FIGURE 26

IP-PARALLEL-IO READ-BACK LOWER BIT MAP

rdbk_u \$38 Parallel Control Register Port read/write

| DATA BIT | Count Data DESCRIPTION |
|----------|------------------------|
| 15-0 | read-back 31-16 |

FIGURE 27

IP-PARALLEL-IO READ-BACK UPPER BIT MAP

Counter/TimerB has a read-back port which allows the count to be read by the host. The count is pipelined and stored into an output register. The register is updated with each count unless the Hold [see base register] bit is set. When the Hold bit is set the output register is disabled from updating; Counter/TimerB continues to count. The register is 32 bits wide. Two reads are required to get the entire 32 bit word via the 16 bit IP data bus. If only the lower or upper words are of interest then the Hold bit can be ignored.

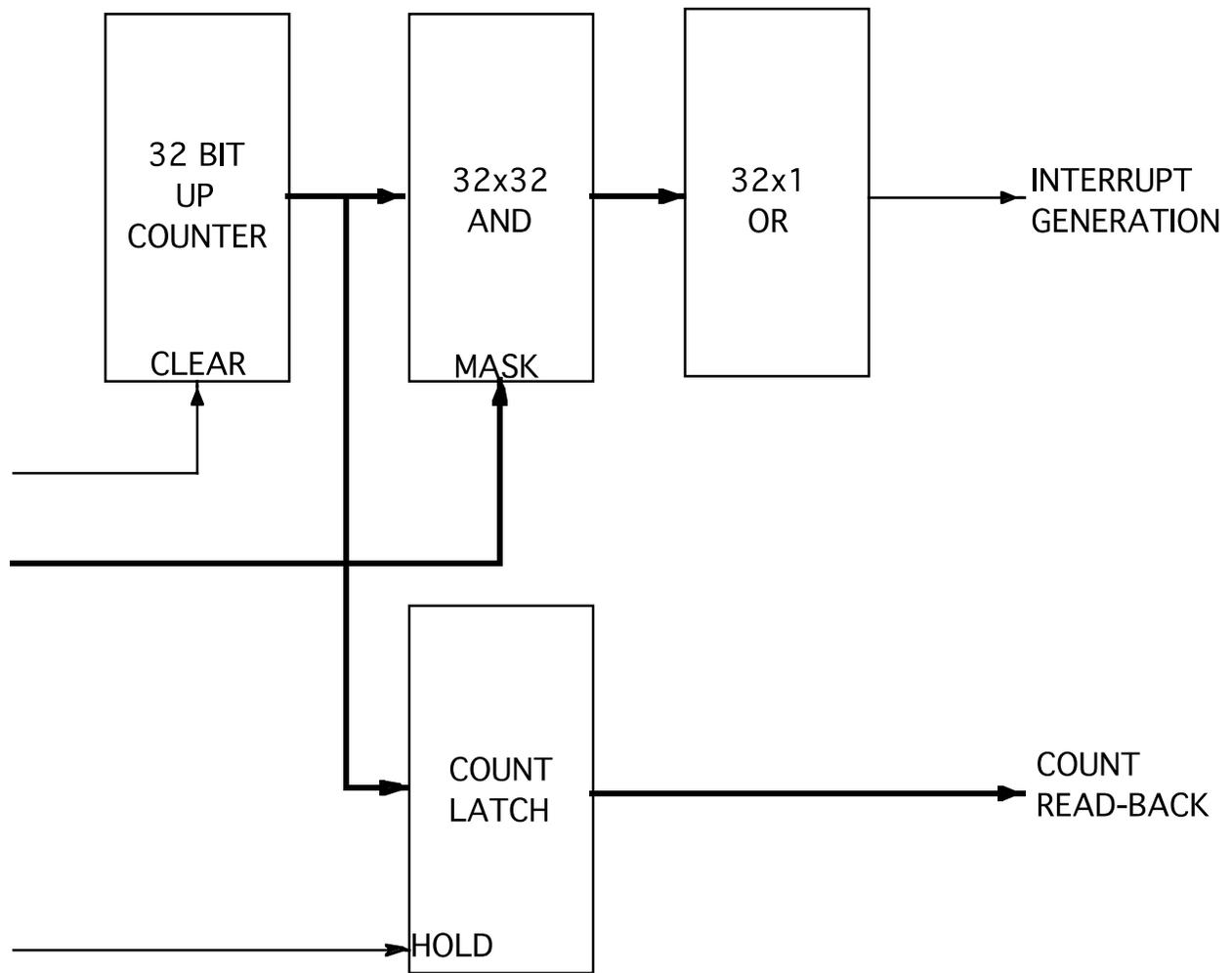


FIGURE 28

IP-PARALLEL-IO COUNTER/TIMER B

Status Register

status \$1E Parallel Status read/write

| Status Register | |
|-----------------|-------------------------------------|
| DATA BIT | DESCRIPTION |
| 15-5 | spare read-only |
| 4 | INTR0 1= interrupt condition active |
| 3 | spare |
| 2 | INTR_DAT 1 = active IO Bit |
| 1 | INTRB 1 = active Counter/TimerB |
| 0 | INTRA 1 = active Counter/TimerA |

FIGURE 29

IP-PARALLEL-IO STATUS BIT MAP

When the interrupt status is set ['1'] then the interrupt event has occurred. If the Interrupt Enable corresponding to the interrupt type and master interrupt enable are set then an interrupt will occur. If the Enable is not set then the interrupt will not be asserted and the status can be used to poll. The Counter/Timer Interrupts are cleared by writing to the status register with the corresponding bit(s) set. Writing to 15-2 will have no affect. The write is transitory – no clear or re-enable is required. The data interrupt is cleared by reading the data from the filtered data ports.

INTR0 is the state of the interrupt condition before the master enable. This bit is useful if operating in a polled mode.

BIS_VECTOR

\$0E Parallel Interrupt Vector Port

The Interrupt vector for the IP-Parallel-IO is stored in this byte wide register. This read/write register is initialized to 'xFF' upon power-on reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered. The interrupt is automatically cleared when the CPU acknowledges the interrupt.



Interrupts

All IP Module interrupts are vectored. The vector from the IP-PARALLEL-IO comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is \$FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-PARALLEL-IO state machines generate an interrupt request when a programmed condition is detected on the IO lines. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector when accessed by the CPU. The source of the interrupt is obtained by reading DATA_IN_FIL0-2. The status remains valid until the registers are read. The interrupt status is auto-cleared when the registers are accessed. The interrupt type can be read from the Status register. There are three interrupt types; Data IO, Counter/Timer A and Counter/Timer B. If both data and timer interrupts are in use then the status register should be read first to determine which interrupt types are active. The exception handler can then respond to all of the current interrupt requests.

Some carrier boards pre-fetch data. If your carrier board pre-fetches the interrupt status, then the status may be cleared when the SW goes to look at it. If this is an issue then be careful with the order of reading the registers to prevent the pre-fetching function from affecting operation.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BASE_CNTL register. The individual enables for IO lines are controllable through INT_EN0-2. The enable operates before the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to read the holding register [DATAIN_FIL0-2], reset the board, or disable the interrupt. The Interrupt acknowledge cycle fetches the vector, but does not clear the interrupt request in this design.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled.



ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision to be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-PARALLEL-IO is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-Parallel-IO board will be recorded with a new code in the DRIVER ID and reserved fields.

| Address | Data | TTL | -1 | -2 | -3 | -4 | -5 | 485 |
|---------|------------------------|------|------|------|------|------|------|------|
| 01 | ASCII "I" | \$49 | \$49 | \$49 | \$49 | \$49 | \$49 | \$49 |
| 03 | ASCII "P" | \$50 | \$50 | \$50 | \$50 | \$50 | \$50 | \$50 |
| 05 | ASCII "A" | \$41 | \$41 | \$41 | \$41 | \$41 | \$41 | \$41 |
| 07 | ASCII "H" | \$48 | \$48 | \$48 | \$48 | \$48 | \$48 | \$48 |
| 09 | Manufacturer ID | \$1E |
| 0B | Model Number | \$03 | \$03 | \$03 | \$03 | \$03 | \$03 | \$03 |
| 0D | Revision | \$A0 |
| 0F | reserved | \$00 | \$00 | \$00 | \$00 | \$00 | \$00 | \$00 |
| 11 | Driver ID, low byte | \$00 | \$00 | \$00 | \$00 | \$00 | \$00 | \$00 |
| 13 | Driver ID, high byte | \$00 | \$01 | \$02 | \$03 | \$04 | \$05 | \$06 |
| 15 | No of extra bytes used | \$0C |
| 17 | CRC | \$68 | \$58 | \$08 | \$38 | \$A8 | \$98 | \$C8 |

FIGURE 30

IP-PARALLEL-IO ID PROM

IP-Parallel-x Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-PARALLEL-IO. Pins marked n/c below are defined by the specification, but not used on the IP-PARALLEL-IO. Also see the User Manual for your carrier board for more information.

| | | | | | |
|--------|------|----------|----|----|--|
| GND | | GND | 1 | 26 | |
| Reset* | CLK | +5V | 2 | 27 | |
| | | R/W* | 3 | 28 | |
| D1 | D0 | IDSEL* | 4 | 29 | |
| | | DMAReq0* | 5 | 30 | |
| D3 | D2 | MEMSEL* | 6 | 31 | |
| | | DMAReq1* | 7 | 32 | |
| D5 | D4 | IntSel* | 8 | 33 | |
| | | DMAAck* | 9 | 34 | |
| D7 | D6 | IOSel* | 10 | 35 | |
| | | n/c | 11 | 36 | |
| D9 | D8 | A1 | 12 | 37 | |
| | | DMAEnd* | 13 | 38 | |
| D11 | D10 | A2 | 14 | 39 | |
| | | n/c | 15 | 40 | |
| D13 | D12 | A3 | 16 | 41 | |
| | | IntReq0* | 17 | 42 | |
| D15 | D14 | A4 | 18 | 43 | |
| | | IntReq1* | 19 | 44 | |
| BS0* | BS0* | A5 | 20 | 45 | |
| BS1* | n/c | n/c | 21 | 46 | |
| | | A6 | 22 | 47 | |
| n/c | n/c | Ack* | 23 | 48 | |
| | | n/c | 24 | 49 | |
| GND | +5V | GND | 25 | 50 | |

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 31

IP-PARALLEL-IO LOGIC INTERFACE

IP-Parallel-IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-IO. Pins marked. Also see the User Manual for your carrier board for more information.

| | | | | |
|-------|-------|--|----|----|
| IO_0 | IO_24 | | 1 | 26 |
| IO_1 | IO_25 | | 2 | 27 |
| IO_2 | IO_26 | | 3 | 28 |
| IO_3 | IO_27 | | 4 | 29 |
| IO_4 | IO_28 | | 5 | 30 |
| IO_5 | IO_29 | | 6 | 31 |
| IO_6 | IO_30 | | 7 | 32 |
| IO_7 | IO_31 | | 8 | 33 |
| IO_8 | IO_32 | | 9 | 34 |
| IO_9 | IO_33 | | 10 | 35 |
| IO_10 | IO_34 | | 11 | 36 |
| IO_11 | IO_35 | | 12 | 37 |
| IO_12 | IO_36 | | 13 | 38 |
| IO_13 | IO_37 | | 14 | 39 |
| IO_14 | IO_38 | | 15 | 40 |
| IO_15 | IO_39 | | 16 | 41 |
| IO_16 | IO_40 | | 17 | 42 |
| IO_17 | IO_41 | | 18 | 43 |
| IO_18 | IO_42 | | 19 | 44 |
| IO_19 | IO_43 | | 20 | 45 |
| IO_20 | IO_44 | | 21 | 46 |
| IO_21 | IO_45 | | 22 | 47 |
| IO_22 | IO_46 | | 23 | 48 |
| IO_23 | IO_47 | | 24 | 49 |
| GND | GND | | 25 | 50 |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 32

IP-PARALLEL-IO IO INTERFACE

IP-Parallel-1 Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-1. Pins marked. Also see the User Manual for your carrier board for more information.

| | | | | |
|--------|--------|--|----|----|
| IO_0 | IO_20 | | 1 | 26 |
| IO_1 | IO_21 | | 2 | 27 |
| IO_2 | IO_22 | | 3 | 28 |
| IO_3 | IO_23 | | 4 | 29 |
| IO_4 | IO_24 | | 5 | 30 |
| IO_5 | IO_25 | | 6 | 31 |
| IO_6 | IO_26 | | 7 | 32 |
| IO_7 | IO_27 | | 8 | 33 |
| IO_8 | IO_28 | | 9 | 34 |
| IO_9 | IO_29 | | 10 | 35 |
| IO_10 | IO_30 | | 11 | 36 |
| IO_11 | IO_31 | | 12 | 37 |
| IO_12 | IO_32 | | 13 | 38 |
| IO_13 | IO_33 | | 14 | 39 |
| IO_14 | IO_34 | | 15 | 40 |
| IO_15 | IO_35 | | 16 | 41 |
| IO_16 | IO_36 | | 17 | 42 |
| IO_17 | IO_37 | | 18 | 43 |
| IO_18 | IO_38 | | 19 | 44 |
| IO_19 | IO_39 | | 20 | 45 |
| IO_40+ | IO_42+ | | 21 | 46 |
| IO_40- | IO_42- | | 22 | 47 |
| IO_41- | IO_43- | | 23 | 48 |
| IO_41+ | IO_43+ | | 24 | 49 |
| GND | GND | | 25 | 50 |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 33

IP-PARALLEL-1 IO INTERFACE

IP-Parallel-2 Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-2. Pins marked. Also see the User Manual for your carrier board for more information.

| | | | | |
|--------|--------|--|----|----|
| IO_0 | IO_16 | | 1 | 26 |
| IO_1 | IO_17 | | 2 | 27 |
| IO_2 | IO_18 | | 3 | 28 |
| IO_3 | IO_19 | | 4 | 29 |
| IO_4 | IO_20 | | 5 | 30 |
| IO_5 | IO_21 | | 6 | 31 |
| IO_6 | IO_22 | | 7 | 32 |
| IO_7 | IO_23 | | 8 | 33 |
| IO_8 | IO_24 | | 9 | 34 |
| IO_9 | IO_25 | | 10 | 35 |
| IO_10 | IO_26 | | 11 | 36 |
| IO_11 | IO_27 | | 12 | 37 |
| IO_12 | IO_28 | | 13 | 38 |
| IO_13 | IO_29 | | 14 | 39 |
| IO_14 | IO_30 | | 15 | 40 |
| IO_15 | IO_31 | | 16 | 41 |
| IO_32+ | IO_36+ | | 17 | 42 |
| IO_32- | IO_36- | | 18 | 43 |
| IO_33- | IO_37- | | 19 | 44 |
| IO_33+ | IO_37+ | | 20 | 45 |
| IO_34+ | IO_38+ | | 21 | 46 |
| IO_34- | IO_38- | | 22 | 47 |
| IO_35- | IO_39- | | 23 | 48 |
| IO_35+ | IO_39+ | | 24 | 49 |
| GND | GND | | 25 | 50 |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 34

IP-PARALLEL-2 IO INTERFACE

IP-Parallel-3 Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-3. Pins marked. Also see the User Manual for your carrier board for more information.

| | | | | | |
|--------|--------|--|----|----|--|
| IO_0 | IO_12 | | 1 | 26 | |
| IO_1 | IO_13 | | 2 | 27 | |
| IO_2 | IO_14 | | 3 | 28 | |
| IO_3 | IO_15 | | 4 | 29 | |
| IO_4 | IO_16 | | 5 | 30 | |
| IO_5 | IO_17 | | 6 | 31 | |
| IO_6 | IO_18 | | 7 | 32 | |
| IO_7 | IO_19 | | 8 | 33 | |
| IO_8 | IO_20 | | 9 | 34 | |
| IO_9 | IO_21 | | 10 | 35 | |
| IO_10 | IO_22 | | 11 | 36 | |
| IO_11 | IO_23 | | 12 | 37 | |
| IO_24+ | IO_30+ | | 13 | 38 | |
| IO_24- | IO_30- | | 14 | 39 | |
| IO_25- | IO_31- | | 15 | 40 | |
| IO_25+ | IO_31+ | | 16 | 41 | |
| IO_26+ | IO_32+ | | 17 | 42 | |
| IO_26- | IO_32- | | 18 | 43 | |
| IO_27- | IO_33- | | 19 | 44 | |
| IO_27+ | IO_33+ | | 20 | 45 | |
| IO_28+ | IO_34+ | | 21 | 46 | |
| IO_28- | IO_34- | | 22 | 47 | |
| IO_29- | IO_35- | | 23 | 48 | |
| IO_29+ | IO_35+ | | 24 | 49 | |
| GND | GND | | 25 | 50 | |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 35

IP-PARALLEL-3 IO INTERFACE

IP-Parallel-4 Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-4. Pins marked. Also see the User Manual for your carrier board for more information.

| | | | | |
|--------|--------|--|----|----|
| IO_0 | IO_8 | | 1 | 26 |
| IO_1 | IO_9 | | 2 | 27 |
| IO_2 | IO_10 | | 3 | 28 |
| IO_3 | IO_11 | | 4 | 29 |
| IO_4 | IO_12 | | 5 | 30 |
| IO_5 | IO_13 | | 6 | 31 |
| IO_6 | IO_14 | | 7 | 32 |
| IO_7 | IO_15 | | 8 | 33 |
| IO_16+ | IO_24+ | | 9 | 34 |
| IO_16- | IO_24- | | 10 | 35 |
| IO_17- | IO_25- | | 11 | 36 |
| IO_17+ | IO_25+ | | 12 | 37 |
| IO_18+ | IO_26+ | | 13 | 38 |
| IO_18- | IO_26- | | 14 | 39 |
| IO_19- | IO_27- | | 15 | 40 |
| IO_19+ | IO_27+ | | 16 | 41 |
| IO_20+ | IO_28+ | | 17 | 42 |
| IO_20- | IO_28- | | 18 | 43 |
| IO_21- | IO_29- | | 19 | 44 |
| IO_21+ | IO_29+ | | 20 | 45 |
| IO_22+ | IO_30+ | | 21 | 46 |
| IO_22- | IO_30- | | 22 | 47 |
| IO_23- | IO_31- | | 23 | 48 |
| IO_23+ | IO_31+ | | 24 | 49 |
| GND | GND | | 25 | 50 |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 36

IP-PARALLEL-4 IO INTERFACE

IP-Parallel-5 Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-5. Pins marked. Also see the User Manual for your carrier board for more information.

| | | | | |
|--------|--------|--|----|----|
| IO_0 | IO_4 | | 1 | 26 |
| IO_1 | IO_5 | | 2 | 27 |
| IO_2 | IO_6 | | 3 | 28 |
| IO_3 | IO_7 | | 4 | 29 |
| IO_8+ | IO_18+ | | 5 | 30 |
| IO_8- | IO_18- | | 6 | 31 |
| IO_9- | IO_19- | | 7 | 32 |
| IO_9+ | IO_19+ | | 8 | 33 |
| IO_10+ | IO_20+ | | 9 | 34 |
| IO_10- | IO_20- | | 10 | 35 |
| IO_11- | IO_21- | | 11 | 36 |
| IO_11+ | IO_21+ | | 12 | 37 |
| IO_12+ | IO_22+ | | 13 | 38 |
| IO_12- | IO_22- | | 14 | 39 |
| IO_13- | IO_23- | | 15 | 40 |
| IO_13+ | IO_23+ | | 16 | 41 |
| IO_14+ | IO_24+ | | 17 | 42 |
| IO_14- | IO_24- | | 18 | 43 |
| IO_15- | IO_25- | | 19 | 44 |
| IO_15+ | IO_25+ | | 20 | 45 |
| IO_16+ | IO_26+ | | 21 | 46 |
| IO_16- | IO_26- | | 22 | 47 |
| IO_17- | IO_27- | | 23 | 48 |
| IO_17+ | IO_27+ | | 24 | 49 |
| GND | GND | | 25 | 50 |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 37

IP-PARALLEL-5 IO INTERFACE

IP-Parallel-485 Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-485. Pins marked. Also see the User Manual for your carrier board for more information. There are 24 pairs of differential signals. IO23-0. See CNTL0-2 and the bit mapping table for more information.

| | | | | | |
|--------|--------|--|----|----|--|
| IO_0+ | IO_12+ | | 1 | 26 | |
| IO_0- | IO_12- | | 2 | 27 | |
| IO_1- | IO_13- | | 3 | 28 | |
| IO_1+ | IO_13+ | | 4 | 29 | |
| IO_2+ | IO_14+ | | 5 | 30 | |
| IO_2- | IO_14- | | 6 | 31 | |
| IO_3- | IO_15- | | 7 | 32 | |
| IO_3+ | IO_15+ | | 8 | 33 | |
| IO_4+ | IO_16+ | | 9 | 34 | |
| IO_4- | IO_16- | | 10 | 35 | |
| IO_5- | IO_17- | | 11 | 36 | |
| IO_5+ | IO_17+ | | 12 | 37 | |
| IO_6+ | IO_18+ | | 13 | 38 | |
| IO_6- | IO_18- | | 14 | 39 | |
| IO_7- | IO_19- | | 15 | 40 | |
| IO_7+ | IO_19+ | | 16 | 41 | |
| IO_8+ | IO_20+ | | 17 | 42 | |
| IO_8- | IO_20- | | 18 | 43 | |
| IO_9- | IO_21- | | 19 | 44 | |
| IO_9+ | IO_21+ | | 20 | 45 | |
| IO_10+ | IO_22+ | | 21 | 46 | |
| IO_10- | IO_22- | | 22 | 47 | |
| IO_11- | IO_23- | | 23 | 48 | |
| IO_11+ | IO_23+ | | 24 | 49 | |
| GND | GND | | 25 | 50 | |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 38

IP-PARALLEL-485 IO INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. Other than series resistors for the “TTL” interface the IP-Parallel does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Integrated circuits can be damaged by static discharge. Proper anti-static handling procedures must be followed.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails.
[\[http://www.dyneng.com/HDRterm50.html \]](http://www.dyneng.com/HDRterm50.html)

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

IndustryPacks® are mezzanine cards which require an adapter to work in any system. IP Modules are commonly used and frequently systems have “extra” slots where the modules can be located. Dynamic Engineering has carriers for the PCI, PCIe, PC104p, VPX, and cPCI buses. IndustryPacks are portable and can be used on third party carriers when the hardware is compliant with the IP specification.

http://www.dyneng.com/pci_3_ip.html

<http://www.dyneng.com/PCIe3IP.html>

<http://www.dyneng.com/pci5ip.html>

<http://www.dyneng.com/PCIe5IP.html>

<http://www.dyneng.com/cpci2ip.html>

<http://www.dyneng.com/cpci4ip.html>

http://www.dyneng.com/pc104p_ip.html

<http://www.dyneng.com/pc104p4ip.html>



<http://www.dyneng.com/VPX2IP.html>

Different platforms have different operating system requirements. If you need a driver please contact Dynamic Engineering. Dynamic Engineering has driver expertise for Windows, Linux, VxWorks. The IP-Parallel series and Dynamic Engineering IP Carriers have drivers available. We can support your effort with driver and application software or help for your software designers. Dynamic Engineering hardware designs have features to help the integrator to write and test their software quickly and efficiently – we can help you.



Loop-back Connections

The ATP software we use to test the IP-Parallel-IO includes a loop-back test. The Engineering Kit for the IP-Parallel-IO includes the source code for the ATP. The loop-back test is facilitated with an IP-Debug-IO card with added wire-wrapped interconnections.

Model “-1” referenced to IP-Parallel-1 Pin Assignment table

TTL loop-back connections

| <u>From</u> | <u>To</u> | <u>Signal</u> |
|-------------|-----------|---------------|
| 1 | 26 | IO0 – IO20 |
| 2 | 27 | IO1 – IO21 |
| 3 | 28 | IO2 – IO22 |
| 4 | 29 | IO3 – IO23 |
| 5 | 30 | IO4 – IO24 |
| 6 | 31 | IO5 – IO25 |
| 7 | 32 | IO6 – IO26 |
| 8 | 33 | IO7 – IO27 |
| 9 | 34 | IO8 – IO28 |
| 10 | 35 | IO9 – IO29 |
| 11 | 36 | IO10 – IO30 |
| 12 | 37 | IO11 – IO31 |
| 13 | 38 | IO12 – IO32 |
| 14 | 39 | IO13 – IO33 |
| 15 | 40 | IO14 – IO34 |
| 16 | 41 | IO15 – IO35 |
| 17 | 42 | IO16 – IO36 |
| 18 | 43 | IO17 – IO37 |
| 19 | 44 | IO18 – IO38 |
| 20 | 45 | IO19 – IO39 |

485 loop-back connections

| | | <u>+side</u> | | | <u>-side</u> |
|----|----|--------------|----|----|--------------|
| 21 | 46 | IO40 – IO42 | 22 | 47 | IO40 – IO42 |
| 24 | 49 | IO41 – IO43 | 23 | 48 | IO41 – IO43 |



Model “-2” referenced to IP-Parallel-2 Pin Assignment table

TTL loop-back connections

| From | To | Signal |
|-------------|-----------|---------------|
| 1 | 26 | IO0 – IO16 |
| 2 | 27 | IO1 – IO17 |
| 3 | 28 | IO2 – IO18 |
| 4 | 29 | IO3 – IO19 |
| 5 | 30 | IO4 – IO20 |
| 6 | 31 | IO5 – IO21 |
| 7 | 32 | IO6 – IO22 |
| 8 | 33 | IO7 – IO23 |
| 9 | 34 | IO8 – IO24 |
| 10 | 35 | IO9 – IO25 |
| 11 | 36 | IO10 – IO26 |
| 12 | 37 | IO11 – IO27 |
| 13 | 38 | IO12 – IO28 |
| 14 | 39 | IO13 – IO29 |
| 15 | 40 | IO14 – IO30 |
| 16 | 41 | IO15 – IO31 |

485 loop-back connections

| | | +side | | | -side |
|----|----|--------------|----|----|--------------|
| 17 | 42 | IO32 – IO36 | 18 | 43 | IO32 – IO36 |
| 20 | 45 | IO33 – IO37 | 19 | 44 | IO33 – IO37 |
| 21 | 46 | IO34 – IO38 | 22 | 47 | IO34 – IO38 |
| 24 | 49 | IO35 – IO39 | 23 | 48 | IO35 – IO39 |



Model “-3” referenced to IP-Parallel-3 Pin Assignment table

TTL loop-back connections

| From | To | Signal |
|-------------|-----------|---------------|
| 1 | 26 | IO0 – IO12 |
| 2 | 27 | IO1 – IO13 |
| 3 | 28 | IO2 – IO14 |
| 4 | 29 | IO3 – IO15 |
| 5 | 30 | IO4 – IO16 |
| 6 | 31 | IO5 – IO17 |
| 7 | 32 | IO6 – IO18 |
| 8 | 33 | IO7 – IO19 |
| 9 | 34 | IO8 – IO20 |
| 10 | 35 | IO9 – IO21 |
| 11 | 36 | IO10 – IO22 |
| 12 | 37 | IO11 – IO23 |

485 loop-back connections

| +side | | | -side | | |
|--------------|----|-------------|--------------|----|-------------|
| 13 | 38 | IO24 – IO30 | 14 | 39 | IO24 – IO30 |
| 16 | 41 | IO25 – IO31 | 15 | 40 | IO25 – IO31 |
| 17 | 42 | IO26 – IO32 | 18 | 43 | IO26 – IO32 |
| 20 | 45 | IO27 – IO33 | 19 | 44 | IO27 – IO33 |
| 21 | 46 | IO28 – IO34 | 22 | 47 | IO28 – IO34 |
| 24 | 49 | IO29 – IO35 | 23 | 48 | IO29 – IO35 |



Model “-4”

TTL loop-back connections

| From | To | Signal |
|-------------|-----------|---------------|
| 1 | 26 | IO0 – IO8 |
| 2 | 27 | IO1 – IO9 |
| 3 | 28 | IO2 – IO10 |
| 4 | 29 | IO3 – IO11 |
| 5 | 30 | IO4 – IO12 |
| 6 | 31 | IO5 – IO13 |
| 7 | 32 | IO6 – IO14 |
| 8 | 33 | IO7 – IO15 |

485 loop-back connections

| +side | | | -side | | |
|--------------|----|-------------|--------------|----|-------------|
| 9 | 34 | IO16 – IO24 | 10 | 35 | IO16 – IO24 |
| 12 | 37 | IO17 – IO25 | 11 | 36 | IO17 – IO25 |
| 13 | 38 | IO18 – IO26 | 14 | 39 | IO18 – IO26 |
| 16 | 41 | IO19 – IO27 | 15 | 40 | IO19 – IO27 |
| 17 | 42 | IO20 – IO28 | 18 | 43 | IO20 – IO28 |
| 20 | 45 | IO21 – IO29 | 19 | 44 | IO21 – IO29 |
| 21 | 46 | IO22 – IO30 | 22 | 47 | IO22 – IO30 |
| 24 | 49 | IO23 – IO31 | 23 | 48 | IO23 – IO31 |



Model “-5” referenced to IP-Parallel-5 Pin Assignment table

TTL loop-back connections

| From | To | Signal |
|-------------|-----------|---------------|
| 1 | 26 | IO0 – IO4 |
| 2 | 27 | IO1 – IO5 |
| 3 | 28 | IO2 – IO6 |
| 4 | 29 | IO3 – IO7 |

485 loop-back connections

| +side | | | -side | | |
|--------------|----|-------------|--------------|----|-------------|
| 5 | 30 | IO8 – IO18 | 6 | 31 | IO8 – IO18 |
| 8 | 33 | IO9 – IO19 | 7 | 32 | IO9 – IO19 |
| 9 | 34 | IO10 – IO20 | 10 | 35 | IO10 – IO20 |
| 12 | 37 | IO11 – IO21 | 11 | 36 | IO11 – IO21 |
| 13 | 38 | IO12 – IO22 | 14 | 39 | IO12 – IO22 |
| 16 | 41 | IO13 – IO23 | 15 | 40 | IO13 – IO23 |
| 17 | 42 | IO14 – IO24 | 18 | 43 | IO14 – IO24 |
| 20 | 45 | IO15 – IO25 | 19 | 44 | IO15 – IO25 |
| 21 | 46 | IO16 – IO26 | 22 | 47 | IO16 – IO26 |
| 24 | 49 | IO17 – IO27 | 23 | 48 | IO17 – IO27 |



Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-PARALLEL-IO is constructed out of 0.062 inch thick High Temp FR4 material.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required. Dynamic Engineering IndustryPack Modules are shipped with a mounting kit.. [IP-MTG-KIT is available if you misplace the mounting hardware or if another IP was not shipped with the standoffs and screws]

The IP Module provides a low temperature coefficient of $0.89 \text{ W}/^{\circ}\text{C}$ for uniform heat. This is based upon the temperature coefficient of the base FR4 material of $0.31 \text{ W}/\text{m}^{\circ}\text{C}$, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.



Thermal Considerations

The IP-Parallel-IO design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options. <http://www.dyneng.com/warranty.html>

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com



Specifications

| | |
|--------------------------|---|
| Logic Interface: | IP Module Logic Interface |
| Features: | Up to 48 open drain IO. 24 mA sink with 10 mA pull-up Up To 24 RS485 Transceivers two counter timers with waveform generator |
| Software Interface: | Control Registers, ID PROM, Vector Register, Status Ports |
| Initialization: | Hardware Reset forces all registers to 0. |
| Access Modes: | Word I/O Space (see memory map) Word in ID Space Vectored interrupt |
| Access Time: | back-to-back cycles in 500ns (8MHz.) or 125 nS (32 MHz.) |
| Wait States: | 1 to all spaces |
| Interrupt: | Multiple interrupt filtering options available on each IO line. Enabled, Active hi or low, edge or level. Two counter/timer programmable interrupts |
| DMA: | No Logic Interface DMA Support implemented at this time. |
| Onboard Options: | All Options are Software Programmable |
| Interface Options: | 50 pin flat cable 50 screw terminal block interface [HDRterm50] User cable |
| Dimensions: | Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches |
| Construction: | FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed. |
| Temperature Coefficient: | 0.89 W/°C for uniform heat across IP |
| Power: | Typical 52 mA @ 5V unloaded. Additional current will be required depending on the loads applied |



Order Information

The IP-Parallel-IO board has 7 standard configurations.

http://www.dyneng.com/ip_parallel_io.html

| | |
|--------|--|
| “-TTL” | 48 TTL IO open drain drivers w/ 470Ω pull-up, 2 counter timers |
| “-1” | 40 TTL and 4 - 485 |
| “-2” | 32 TTL and 8 - 485 |
| “-3” | 24 TTL and 12 - 485 |
| “-4” | 16 TTL and 16 – 485 |
| “-5” | 8 TTL and 20 – 485 |
| “-485” | 24 - 485 |



Tools for IP-PARALLEL-IO

IP-Debug-Bus - IP Bus interface extender with testpoints, isolated power & quickswitch technology to allow hot swapping or power cycling without powering down the host.

<http://www.dyneng.com/ipdbgbus.html>

IP-Debug-IO II - IndustryPack IO connector breakout with testpoints, ribbon cable headers, and locations for user circuits.

<http://www.dyneng.com/ipdbgio.html>

HDRterm50 - Ribbon cable compatible 50 pin header to 50 screw terminal header. Comes with DIN rail mounting capability.

<http://www.dyneng.com/HDRterm50.html>

HDRribn50 – Ribbon cable in several standard lengths plus custom, with strain relief and cable pull attached.

<http://www.dyneng.com/HDRribn50.html>

PCI3IP - 1/2 length PCI card with 3 IP slots.

http://www.dyneng.com/pci_3_ip.html

PCle3IP - 1/2 length PCIe card with 3 IP slots.

<http://www.dyneng.com/PCle3IP.html>

PCI5IP - PCI card with 5 IP slots.

<http://www.dyneng.com/pci5ip.html>

PCle5IP - PCIe card with 5 IP slots.

<http://www.dyneng.com/PCle5IP.html>

cPCI2IP - cPCI card with 2 IP slots.

<http://www.dyneng.com/cpci2ip.html>

cPCI4IP - cPCI card with 4 IP slots.

<http://www.dyneng.com/cpci4ip.html>

PC104pIP - PC104p card with 1 IP slot.

http://www.dyneng.com/pc104p_ip.html

PC104p4IP - PC104p card with 4 IP slots.

<http://www.dyneng.com/pc104p4ip.html>

IP-MTG-KIT – 4 metric stainless screw and stand-off pairs to retain IP-Parallel-IO against the carrier board. Flat head screws match IP Specification mounting requirements.

<http://www.dyneng.com/IPHardware.html>

All information provided is Copyright Dynamic Engineering

