User Manual

Hardware Description

Maxwell-2

Manual Revision 01p0
Revision Date 2/6/2023

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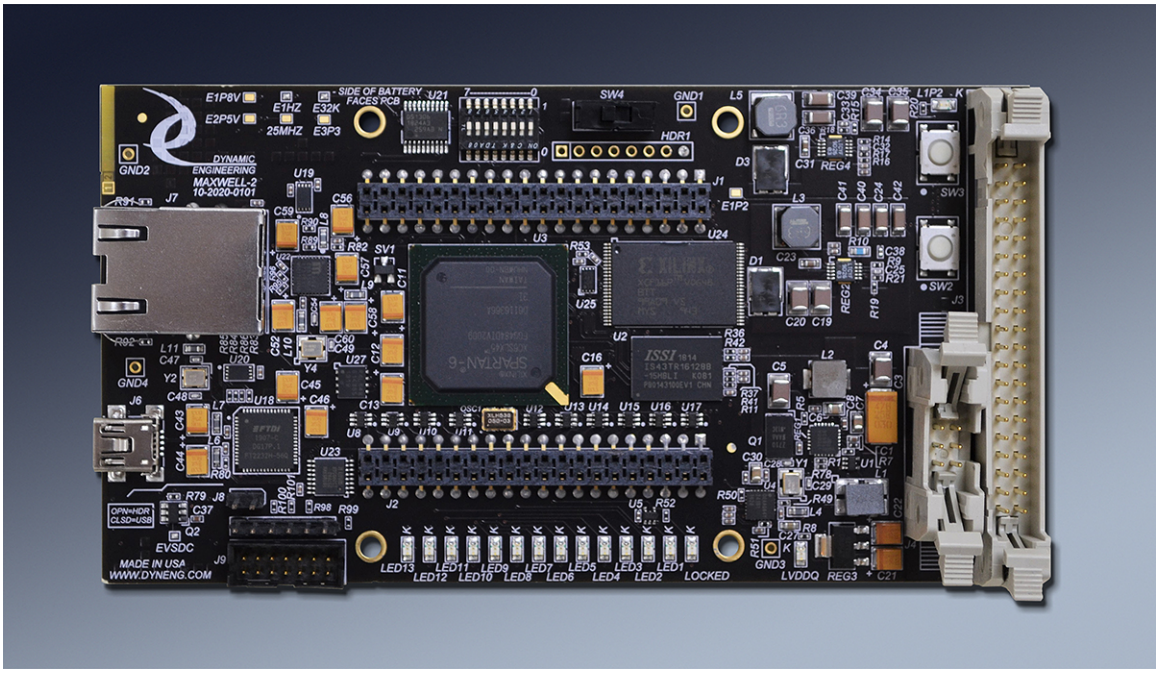
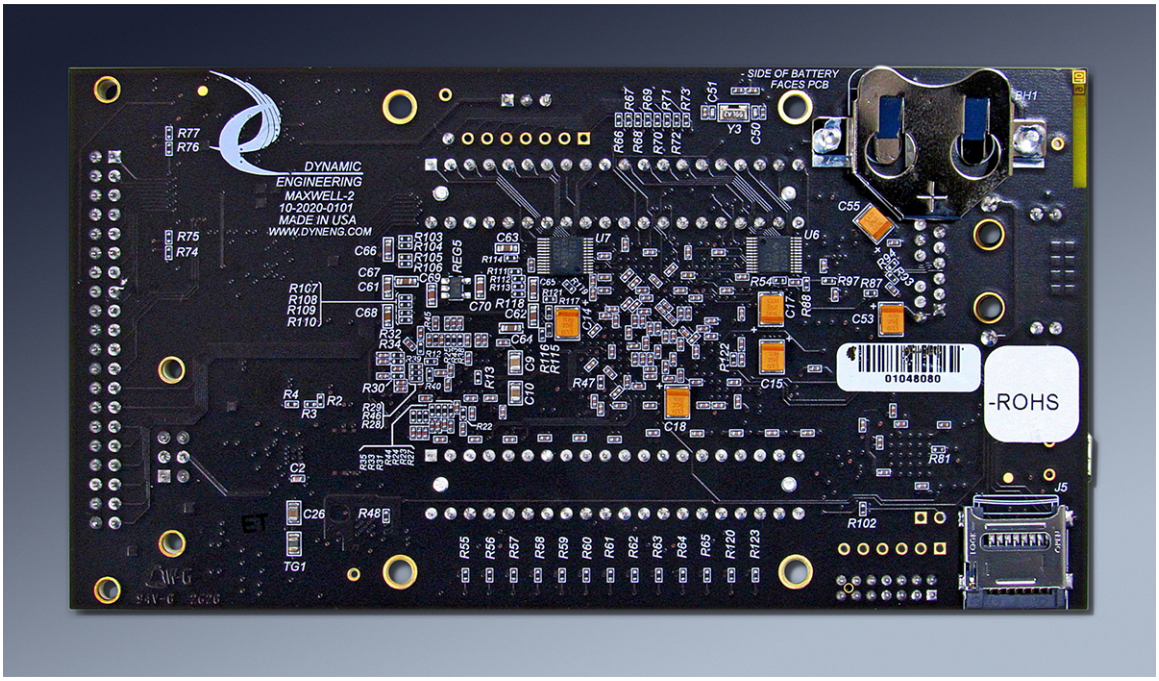
Primary View



Corresponding Hardware: 10-2020-0102

Rear View



Cautions and Warnings

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at their own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without express written approval from the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

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Design Revision History

Table 1: Flash and Software Revision History

Revision	Date	Description
Flash		
1.0	7/2020	Initial release
1.4	12/2023	Updated for Revision 2 of the PCB
		PCB
01 02 03	7/20 9/20 1/23	Initial Release Incorporate jumpers Replace SD Card with on board FLASH

Manual Revision History

Table 2: Manual Revision History

Revision	Date	Description
01p0	01/03/23	Initial release of manual

NOTE: Dynamic Engineering has made every effort to ensure that this manual is accurate and complete; that being said, the company reserves the right to make improvements or changes to the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

Key Product Features

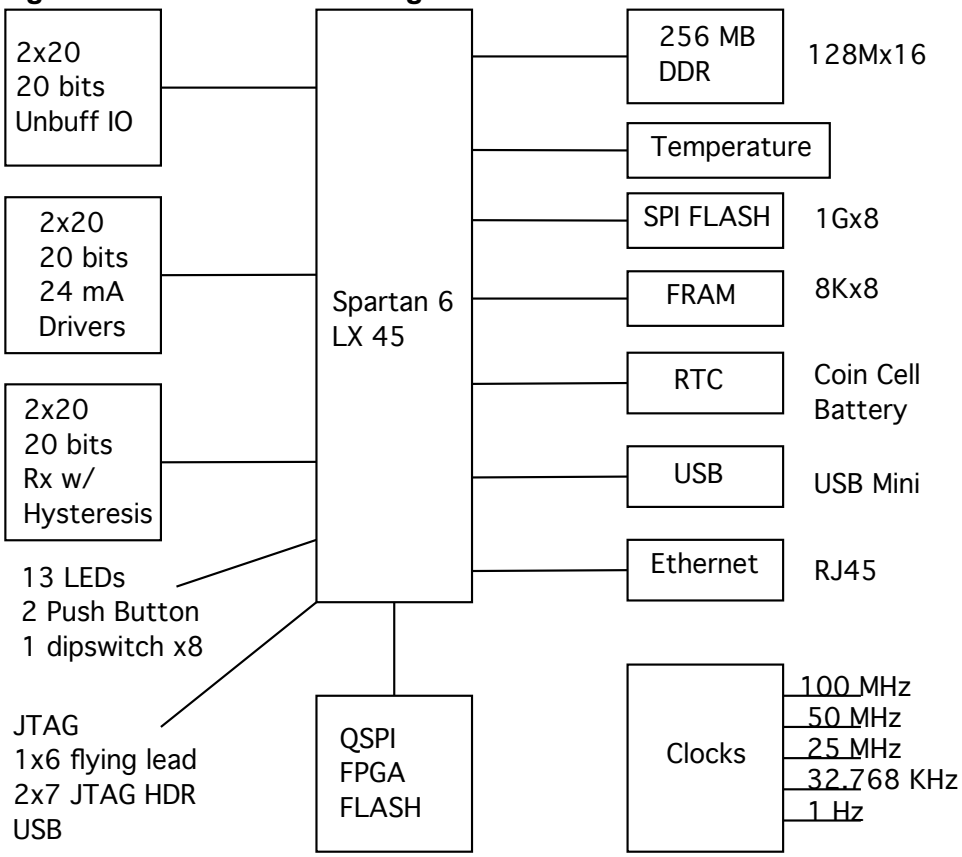
Maxwell-2 provides a user programmable FPGA with common support elements. The Spartan 6 45 provides the controlling logic and features a MicroBlaze processor built into the fabric. 5V and Ground are converted to the internal voltages required to operate all of the internal devices. Multiple parallel ports, USB, Ethernet, FRAM, DDR, RTC with battery back-up, and several clock references are supplied. New with revision 03 is the addition of SPI FLASH.

Store your VHDL/ Verilog design plus initial boot code for the ARM in the QSPI to load automatically at power up. Store / load additional SW and data with the FLASH, USB, or Ethernet interfaces. Program the QSPI direct with the programming header or use the USB port to interconnect. Store user parameters, status information, configuration etc. into the FRAM. Separate [not shown] configuration storage for the Ethernet and USB ports.

Use as part of an embedded system, standalone device, a development or test tool. Industrial temperature devices with an option for conformal coating if needed. Low power dissipation – typical .5A@5V in standby with DDR refreshing, FPGA operating and waiting for commands.

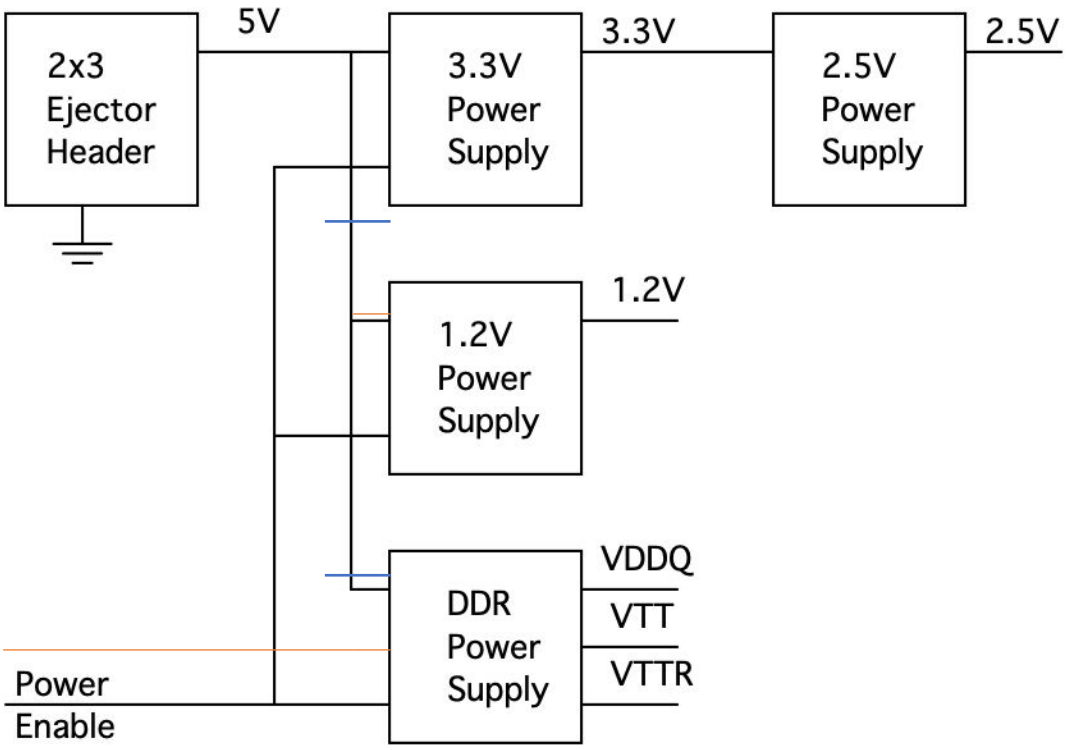
Contact us if you need a variant with different IO etc.

Figure 1: Maxwell-2 block diagram



Product Description

Figure 2: Maxwell-2 Power Distribution Diagram



To support SW and hardware centric designs 128Mx16 of DDR is attached to the memory controller. The DDR can be used to support HW based designs – configured as a FIFO or RAM etc. The DDR can support the ARM as the main operational memory to support the processor.

QSPI supplies the initial configuration for the FPGA including the initialization software. As part of the initialization process the application program can be moved from FLASH to DDR for operation. Small designs can fit within the QSPI memory.

SPI FLASH 1Gx8 in organization is provided for larger storage requirements without using external devices. The interface is configured as 4 bit parallel – QSPI – and rated to 120 MHz. The reference design includes a FIFO based interface to allow full rate page reads and writes to be processed as well as single word read/write operations. Since the FLASH is larger than the DDR several revisions / versions can be kept within the FLASH. The supplied DIP switch can be read and used to select which portion of the FLASH is loaded [user option].

The temperature of the PCB near the FPGA is available via the temperature port. LM75BTP is the device utilized in this design. The base design available in the engineering kit includes a register based I2C interface to the temperature sensor. 11 bit accuracy over the -55C to +125C range. The

over temperature alarm can be programmed and used as an alert within the FPGA.

FRAM is also I2C based and has a separate bus also with register interface. The separate bus allows the temperature to be read in parallel with read/write operations to FRAM. The FRAM is 8Kx8 in organization.

Real Time Clock is based on DS1306EN with a direct interface to the FPGA. The RTC is supported with a 20 mm coin cell located at the card edge. 32.768 KHz. is the reference crystal frequency. Two interrupts and two clock outputs are tied back to the FPGA. The clocks also go to test points. The RTC is accessed with a SPI interface. A separate register interface is provided to interact with the interface and to program and read back the time.

USB is implemented with a bridge. The FPGA side of the interface looks like a UART. USB Mini B on the IO side. FT2232H is the device in use. Supported with 1K bit EEP. 12 MHz crystal for the reference.

Ethernet is also implemented with a bridge. The FPGA side of the interface is SPI, RJ45 on the IO side. 10/100 interface. 1K EEPROM for configuration. 25 MHz crystal. LEDs at RJ45 under bridge control with programming options within bridge. LED0 connected to Left LED, LED1 connected to Right LED.

Three 20 bit Parallel ports are supplied. One port is unbuffered, bidirectional. “J3” at the top of the Maxwell-2. Since directly connected to the FPGA it is recommended to use this port for inside the chassis wiring situations. This port has a standard locking header 2x20.

The Input Port “J2” has 22 ohm series protection resistors on Revision 2 and hysteresis receivers for revision 3. This port is implemented with a 2x20 socket. .1” pitch.

The output port “J1” is supported with 24 mA buffers. This port also has 2x20 socket as the connector. 1” pitch.

There are 13 user LEDs available to the designer. Simple register interface to control. Recommend open drain definitions – float off, low on for the control.

DIPSWITCH is an 8-segment slide switch with user defined application. The switch can be used to control how the system behaves at power up, make operational selections, etc.

PB1 & PB2 The two push-button inputs can be used to gain the local processors attention for user defined purposes.

Power Supplies are built in to create the required voltages to operate the FPGA, DDR, USB, Ethernet, RTC etc. The supplies are implemented as DC/DC converters. Each has filtering appropriate to the loads connected. In addition, the devices are properly bypassed and have bulk decoupling at the load. Planes are used for power distribution and double as thermal averaging across the board to allow the entire board to act as a heat sink.

Product Specifications

Table 3: Product Specifications

Specification	Description
Memory	1Gx8 SPI FLASH, 256 MB DDR, 8Kx8 FRAM, additional block RAM within FPGA
Ports	RTC, USB, Etherent, 20 bit parallel out, 20 bit parallel in, 20 bit parallel unbuffered
CPU	MicroBlaze within FPGA fabric
LEDs	13 User LEDs
FLASH	QSPI initial storage, QSPI FLASH for expanded program storage
Temperature	Industrial temperature components
Connectors	USB mini, Ethernet RJ45, Parallel port headers
FPGA	Spartan VI 45 484

Construction and Reliability

Dynamic Engineering Modules are conceived and engineered for rugged industrial environments. Maxwell is constructed out of 0.062-inch thick High-Temp RoHS-compliant FR4 material.

RoHS and standard processing are available options.

Through-hole and surface-mount components are used. Locking headers for Power and bi-directional port. Keyed connectors for USB and Ethernet.

Mounting positions are provided to secure Maxwell to another surface or for stand-offs or other “feet” to be installed as desired.

The PCB provides a (typical based on PMC) low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the board. The coefficient means that if 2.17 Watts are applied uniformly on the component side, the temperature difference between the component side and solder side is one degree Celsius.

Installation and Interfacing Guidelines

Some general interfacing guidelines are presented below. If you need more assistance, contact Dynamic Engineering.

Installation

Warning: Connection of incompatible hardware is likely to cause serious damage.

ESD

Proper ESD handling procedures must be followed when handling Maxwell. The cards are shipped in anti-static shielded bags. The cards should remain in their bags until ready to use. When installing the

card, the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-Up

Guidelines

Grounds

All electrically grounded equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power Supply

Inputs can be damaged by static discharge or by applying voltage outside of the device-rated voltages.

Thermal Considerations

The Maxwell design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading; forced-air cooling is recommended. With the one-degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Theory of Operation

Maxwell is a user implemented control board with processing, IO, FPGA capabilities. As such the design is not “plug and play” until the design work has been accomplished. The design may or may not use all of the features of Maxwell. For example, It is very reasonable to not use the ARM and have a HW implementation utilizing the various ports. Our test set-up uses the bidirectional parallel port to implement a SPI interface and an external device to control the various ports for ATP purposes. If you want to do a HW implementation or perhaps a SPI expansion of this sort we can provide the test VHDL set to get your project started.

If using the MicroBlaze CPU the design will likely be done in the Vivado. The AXI interconnects can be used to connect to SPI controllers to communicate with the external IO, parallel ports for the parallel ports or the memory management unit for the DDR. Alternatively, the decoder can be used and standard VHDL blocks used to interface with the hardware. Depending on your preference a block diagram approach or more direct implementation can be performed. Once the design is captured the software to run on the embedded RISC processor can be merged or implemented, compiled along with the hardware and stored into the QSPI to initialize and run.

Dynamic Engineering plans to develop a start configuration to allow clients to develop SW with the rest of the structure already in place. You will be able to add your own internal accelerators, filters, expanded HW interfaces with our design providing the running start.

Connector Definitions

In addition to connectors the switches are also covered in this section

Table 4: J4 Power Connector

Pin Number	Description
1,2,5,6	Ground
3,4	5V

J4 is a locking 2x3 .1” standard header with keying. The center pins are power and the corner pins are ground making the connector alignment proof. The locking mechanism will both retain the cable and serve as an ejector to aide in removing the power cable.

The 5V and Ground reference are filtered with a Common Mode Bead with a 5A rating. In addition, a transorb set to 5.6V protects the internal circuitry. Not meant for constant over-voltage protection [momentary with .1J rating]

Table 5: J1 Parallel Output Connector

Pin Number	Description
1	IDC_OUT1
3	IDC_OUT2
5	IDC_OUT3
7	IDC_OUT4
9	IDC_OUT5
11	IDC_OUT6
13	IDC_OUT7
15	IDC_OUT8
17	IDC_OUT9
19	IDC_OUT10
21	IDC_OUT11
23	IDC_OUT12
25	IDC_OUT13
27	IDC_OUT14
29	IDC_OUT15
31	IDC_OUT16
33	IDC_OUT17
35	IDC_OUT18
37	IDC_OUT19
39	IDC_OUT20
2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40	Ground

J1 is a 2x20 socket connector with .1” spacing. Alternate pins are ground as shown. The Output signals originate at the FPGA and are buffered with a +/-24 mA driver with 3.3V reference. Depending on the load the output voltage will approach 3V. Single ended, non-inverted, LVTTL voltage range.

Table 6: J2 Parallel Input Connector

Pin Number	Description
1	IDC_IN1
3	IDC_IN2
5	IDC_IN3
7	IDC_IN4
9	IDC_IN5
11	IDC_IN6
13	IDC_IN7
15	IDC_IN8
17	IDC_IN9
19	IDC_IN10
21	IDC_IN11
23	IDC_IN12
25	IDC_IN13
27	IDC_IN14
29	IDC_IN15
31	IDC_IN16
33	IDC_IN17
35	IDC_IN18
37	IDC_IN19
39	IDC_IN20
2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40	Ground

J2 is a 2x20 socket connector with .1” spacing. Alternate pins are ground as shown. The received signals are routed to the FPGA. Revision 2 PCB utilizes 22 ohm series resistors. Revision 3 and later incorporate hysteresis buffers [‘17]. LVTTL is the expected input voltage. Standard single gate load per signal.

Table 7: J3 Parallel IO Connector

Pin Number	Description
1	IDC_IO1
3	IDC_IO2
5	IDC_IO3
7	IDC_IO4
9	IDC_IO5
11	IDC_IO6
13	IDC_IO7
15	IDC_IO8
17	IDC_IO9
19	IDC_IO10
21	IDC_IO11
23	IDC_IO12
25	IDC_IO13
27	IDC_IO14
29	IDC_IO15
31	IDC_IO16
33	IDC_IO17
35	IDC_IO18
37	IDC_IO19
39	IDC_IO20
2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40	Ground

J3 is a 2x20 locking header connector with .1” spacing. Alternate pins are ground as shown. The signals are routed directly to the FPGA. Care must be used with this interface as it does not have any protection against ESD, over voltage etc. Since this port is un-buffered each IO can be used as an input, output or as a bidirectional signal. J3 is located across the top of the card near the power connector.

Table 8: H1 JTAG Connector

Pin Number	Description
1	3.3V
2	Ground
3	TCK
4	TDO
5	TDI
6	TMS

H1 is a 1x6 header position [un-populated]. The pin definitions align with the USB Platform Cable adapter commonly used with Xilinx. Using the “flying leads” configuration one can connect to a 1x6 header and push into the board to make contact allowing for quick connect and disconnect.

Table 9: J9 JTAG Connector

Pin Number	Description
2	3.3V
3,5,7,9,11,13	Ground
6	TCK
8	TDO
10	TDI
4	TMS

J9 is an alternate parallel connected 2x7 2 mm header. The pin definitions align with the ribbon cable adapter commonly used with Xilinx. Pins 1,12, 14 are not used.

The combined JTAG interface is routed through a mux to the FPGA to allow programming of the QSPI memory or to load a bit file directly into the FPGA. The mux is controlled with J8. When J8 is open either H1 or J9 can be used. When J8 has a shunt installed the USB port can be used to program the memory. The B port is used for this purpose.

SW1 is the Dipswitch. The dipswitch is tied to 3.3V with 4.7K pull-up resistors. When the switches are closed the ground over-rides the pull-up. In parallel with the Dipswitch connections is **HDR1**. HDR1 is a 1x8 .1" spacing header [not installed]. If the Dipswitches are in the "open" position the signals can be driven rather than read to create 8 test points without using up parallel port IO. Handy for integration when you need to see the state of internal signals.

SW2 and **SW3** are the two pushbutton switches. Both are momentary with the open position '1' and closed = '0' effectively inverting. The switches are for user purposes.

SW4 is the power slide switch. When in the on position [switch toward pin 3] the power supplies are enabled. When toward pin 1 the power supplies are disabled. Please note: this function is accomplished at the regulator shut-down and run pins [active high to enable operation]. The regulators are still running the output is just disabled. The current from the reference supply is greatly reduced but not "zero" in this mode. Shut off at the supply for a true off condition.

Warranty and Repair

Please refer to the warranty page on our website for the warranty and options that are currently offered.

www.dyneng.com/warranty

Service Policy

Before returning a product for repair, verify to the best of your ability, that the suspected unit is as fault. Then call the Dynamic Engineering Customer Service Department for a Return Material Authorization (RMA) number. Carefully package the product, in the original packaging if possible, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by anyone other than the original customer will be treated as out-of-warranty.

Out-of-Warranty Repairs

Out-of-warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the list price for one of that kind of unit. Return transportation and insurance will be billed as part of the repair in addition to the minimum RMA charge.

Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite B/C
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(831) 457-8891
support@dyneng.com

Ordering Information

Industrial Temperature Rated Components: -40 - 85°C

Table 10: Ordering Information

Product	Description
	Maxwell-2.
	FPGA – Spartan 6-45 with MicroBlaze processor. QSPI FLASH configuration memory and user storage, DDR, Ethernet, USB, RTC, Temperature Sensor, Parallel ports (3), LEDs, Power Supplies, Dip and momentary switches.
	Options: Standard or -ROHS assembly AC adapter for Maxwell -CC Conformal Coating

Glossary

Baud	Used as the bit period when talking about UARTs; Not strictly correct, but is the common usage when talking about UARTs.
CardID	Unique number assigned to a design to distinguish between all designs of a particular vendor
CFM	Cubic feet per minute
FIFO	First In First Out memory
Flash	Non-volatile memory used on Dynamic Engineering boards to store FPGA configurations or BIOS
JTAG	Joint Test Action Group – a standard used to control serial data transfer for test and programming operations.
LFM	Linear feet per minute
LVDS	Low Voltage Differential Signaling
MUX	Multiplexor – multiple signals multiplexed to one with a selection mechanism to control which path is active.
Packed	When UART characters are always sent/received in groups of four, allowing full use of host bus/FIFO bandwidth.
Packet	Group of characters transferred. When the characteristics of the group of characters is known, the data can be stored in packets and transferred as such; the system is optimized as a result. Any number of characters can be transferred.
PCI	Peripheral Component Interconnect – parallel bus from host to this device
PIM	PMC Interface Module (PIM). Provides rear I/O in cPCI systems. Mounts to PIM Carrier
PIM Carrier	PIM Mounting Device. Mounts on rear of cPCI backplane.
PMC	PCI Mezzanine Card – establishes common connectors, connections, size and other mechanical features.
TAP	Test Access Port – basically a multi-state port that can be controlled with JTAG [TMS, TDI, TDO, TCK]. The TAP States are the states in the State Machine that are controlled by the commands received over the JTAG link.
TCK	Test Clock provides synchronization for the TDI, TDO, and TMS signals

TDI	Test Data in – this serial line provides the data input to the device controlled by the TMS commands. For example, the data to program the FLASH comes on the TDI line while the commands to the state machine to move through the necessary states comes over TMS. Rising edge of TCK valid.
TDO	Test Data Out is the shifted data out. Valid on the falling edge of the TCK. Not all states output data.
TMS	Test Mode State – this serial line provides the state switching controls. '1' indicates to move to the next state, '0' means stay put in cases where delays can happen; otherwise, 0,2 are used to choose which branch to take. Due to the complexity of state manipulation, the instructions are usually precompiled. Rising edge of TCK valid.
UART	Universal Asynchronous Receiver Transmitter. Common serialized data transfer with start bit, stop bit, optional parity, optional 7/8 bit data. Can be over any electrical interface. RS232 and RS422 are most common.
Unpacked	When UART characters are sent on an unknown basis requiring single character storage and transfer over the host bus
VendorID	Manufacturers number for PCI/PCIe boards. DCBA is Dynamic Engineering's VendorID
VME	Versa Module European
VPX	Family of standards based on the VITA 46.0
XMC	Switched mezzanine card (PMC with PCIe)