DYNAMIC ENGINEERING
150 DuBois St. Suite B&C, Santa Cruz, CA. 95060
831-457-8891 sales@dyneng.com
www.dyneng.com
Est. 1988

User Manual

PC104p-BaseBoard

PC104p Stack
35 Optocoupled Inputs
37 Optocoupled Outputs
2 UART – RS-485 ports
2 ARINC 429 – TX/RX
4 ADC Ports
4 DAC Ports

Revision 2p1
Corresponding Hardware: 10-2005-0102/3

PC104p-BaseBoard
PC104p Stack
Optocoupled Inputs
Optocoupled Outputs
UART ports
ARINC 429
A/D, D/A

Dynamic Engineering
150 DuBois St.
Suite B&C
Santa Cruz, CA 95060
831-457-8891

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PC/104p Modules and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised 12/21/23

Table of Contents

PRODUCT DESCRIPTION 6

ADDRESS MAP 12

PROGRAMMING 14

REGISTER DEFINITIONS 15

BB_BASE 15
BB_WD3, BB_WD4, BB_WD5 17
BB_WD1 18
BB_WD2 19
BB_WD6 20
BB_WD1_CLK, BB_WD2_CLK, BB_WD6_CLK 21
BB_Wdx_y 22
BB_WD1_INT 23
BB_WD2_INT 24
BB_WD6_INT 25
429 Ports 27
3282 Control Bit Description 28
BB_429_INT 31
BB_UART0_CNTL,BB_UART1_CNTL 33
BB_UART0,BB_UART1 35
BB_AN_STAT 35
BB_DACx 36
BB_ADCx 36

Interrupts 37

WORD ⇔ CONNECTOR DEFINITIONS 38

Pin assignments for Word 1 38

Pin assignments for Word 2 38

Pin assignments for Word 3 39

Pin assignments for Word 4 40

Pin assignments for Word 5 40

Pin assignments for Word 6 41

Pin assignments for UART, ADC, DAC, 429 42

Pin assignments for Power, GND 43

APPLICATIONS GUIDE 44

Interfacing 44

CONSTRUCTION AND RELIABILITY 45

THERMAL CONSIDERATIONS 45

WARRANTY AND REPAIR 46

SERVICE POLICY 46

OUT OF WARRANTY REPAIRS 46

FOR SERVICE CONTACT: 46

SPECIFICATIONS 47

ORDER INFORMATION 48

List of Figures

FIGURE 1	BASEBOARD PICTURE	6
FIGURE 2	BASEBOARD BLOCK DIAGRAM	7
FIGURE 3	BASEBOARD INTERNAL ADDRESS MAP	13
FIGURE 4	BASEBOARD BASE CONTROL REGISTER BIT MAP	15
FIGURE 5	BASEBOARD OUTPUT WORD REGISTER BIT MAP	17
FIGURE 6	BASEBOARD WORD 1 BIT MAP	18
FIGURE 7	BASEBOARD WORD 2 BIT MAP	19
FIGURE 8	BASEBOARD WORD 6 BIT MAP	20
FIGURE 9	BASEBOARD TX CONTROL BIT MAP	21
FIGURE 10	BASEBOARD RX BIT CONTROL MAPS	22
FIGURE 11	BASEBOARD INTERRUPT WORD1 BIT MAP	23
FIGURE 12	BASEBOARD INTERRUPT WORD2 BIT MAP	24
FIGURE 13	BASEBOARD INTERRUPT WORD6 BIT MAP	25
FIGURE 14	BASEBOARD 429 AND UART STATUS REGISTER	31
FIGURE 15	BASEBOARD UART CONTROL BIT MAP	33
FIGURE 16	BASEBOARD UART BIT MAP	35
FIGURE 17	BASEBOARD ANALOG STATUS BIT MAP	35
FIGURE 18	BASEBOARD WORD1 CONNECTOR DEFINITION	38
FIGURE 19	BASEBOARD WORD2 CONNECTOR DEFINITION	38
FIGURE 20	BASEBOARD WORD3 CONNECTOR DEFINITION	39
FIGURE 21	BASEBOARD WORD4 CONNECTOR DEFINITION	40
FIGURE 22	BASEBOARD WORD5 CONNECTOR DEFINITION	40
FIGURE 23	BASEBOARD WORD6 CONNECTOR DEFINITION	41
FIGURE 24	BASEBOARD UART, 429, ADC, DAC CONNECTOR DEFINITION	42
FIGURE 25	BASEBOARD POWER & GND CONNECTOR DEFINITION	43

Product Description

PC104p-BaseBoard is part of the PC/104 Module family of modular I/O components by Dynamic Engineering. PC104p-BaseBoard “BaseBoard” is used to integrate a PC/104p stack with the power supply, OptoCoupled inputs and outputs, ARINC 429 IO, UART IO and analog IO. The righthand PC/104 slot is designed to be occupied by the Power Supply module which accepts 28V and supplies the standard PC/104 voltages on the ISA connector. The lefthand slot in Figure 1 is used to add a PC/104p stack. The PC/104p stack will include the system CPU in the system.

The BaseBoard functions occupy slot position 0.

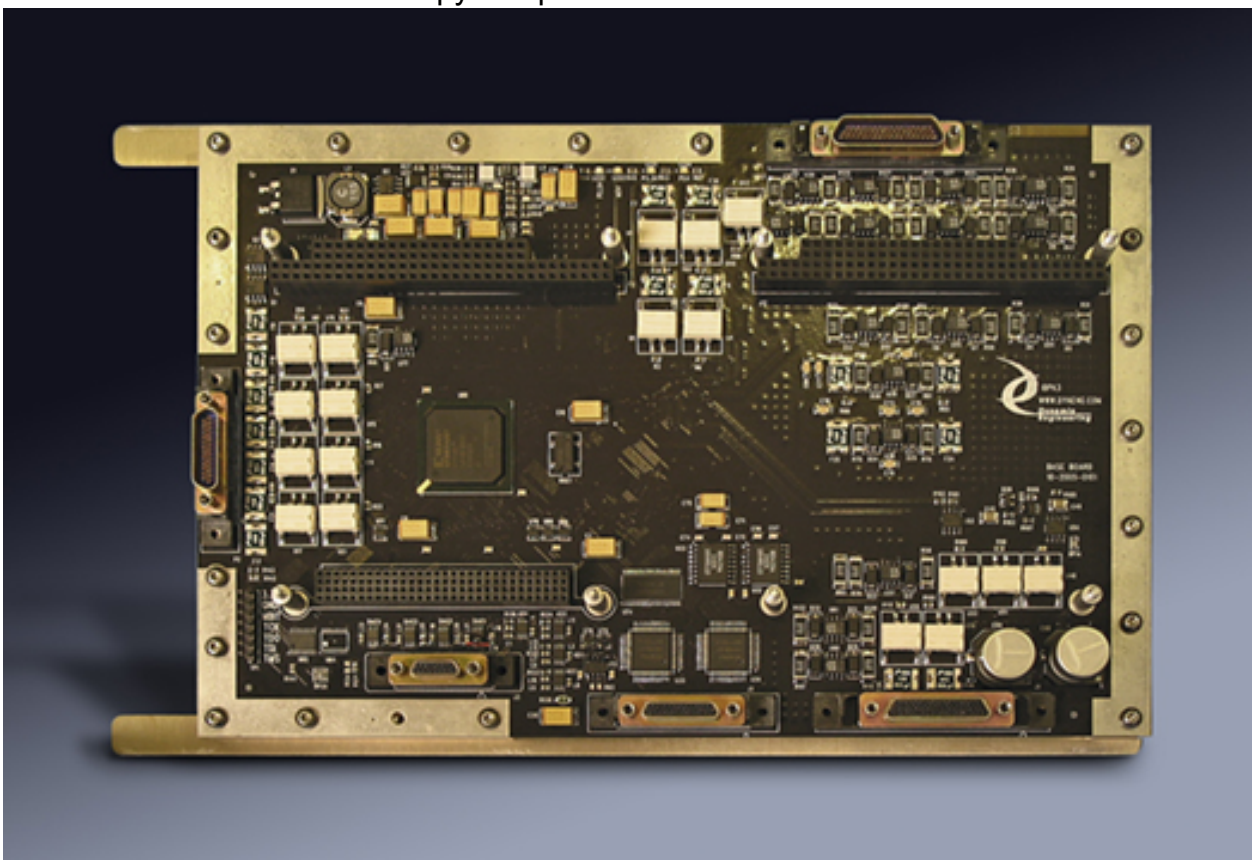


FIGURE 1 BASEBOARD PICTURE

The PC/104p-BaseBoard is shown mounted to the lower plate of the chassis.

The BGA device on the left side is a Xilinx Spartan III [FPGA]. The Xilinx interfaces with the host computer via the PCI bus and provides the local decoding, filtering, specialized bus interfaces etc. The Xilinx is programmed using FLASH memory. The FLASH is supported with a JTAG header for ease of upgrades.

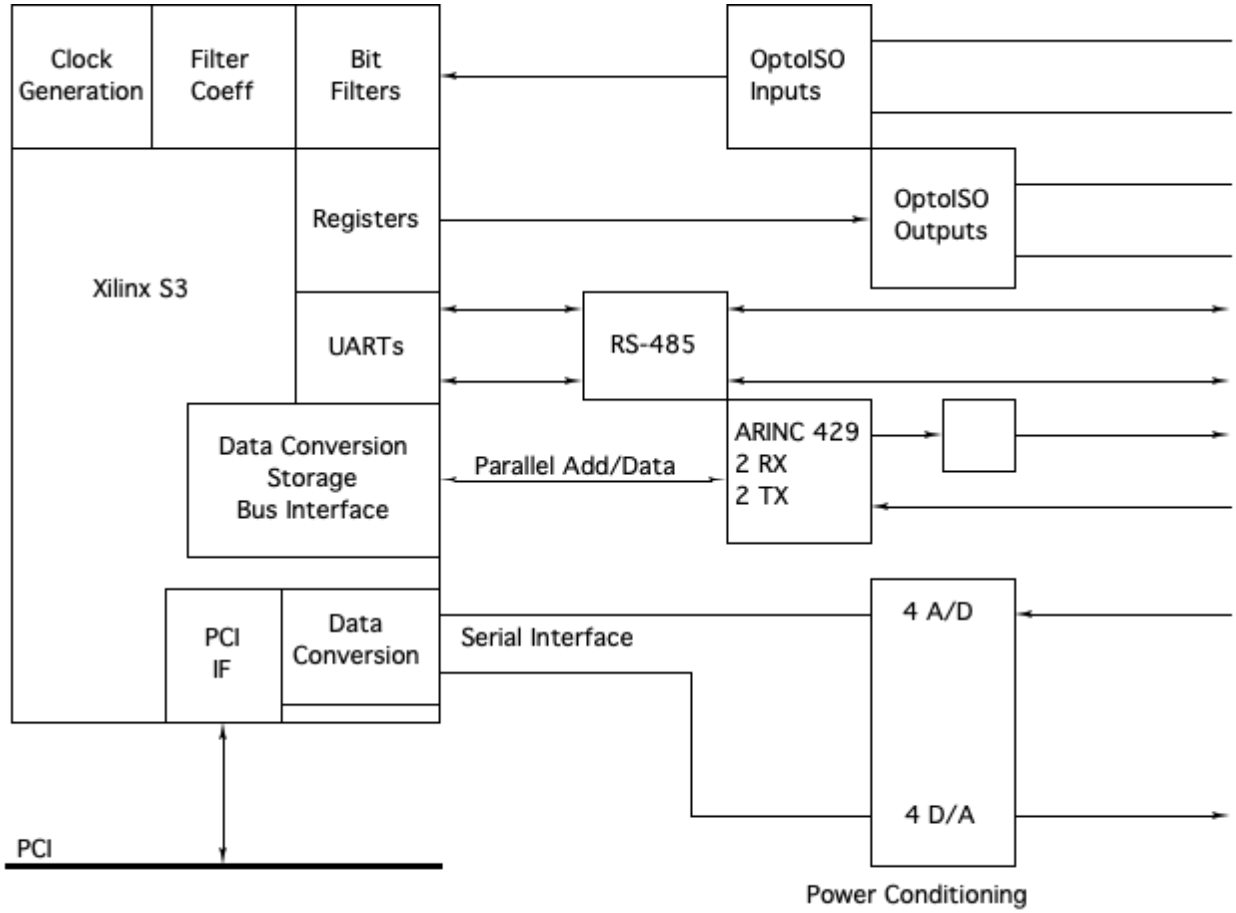
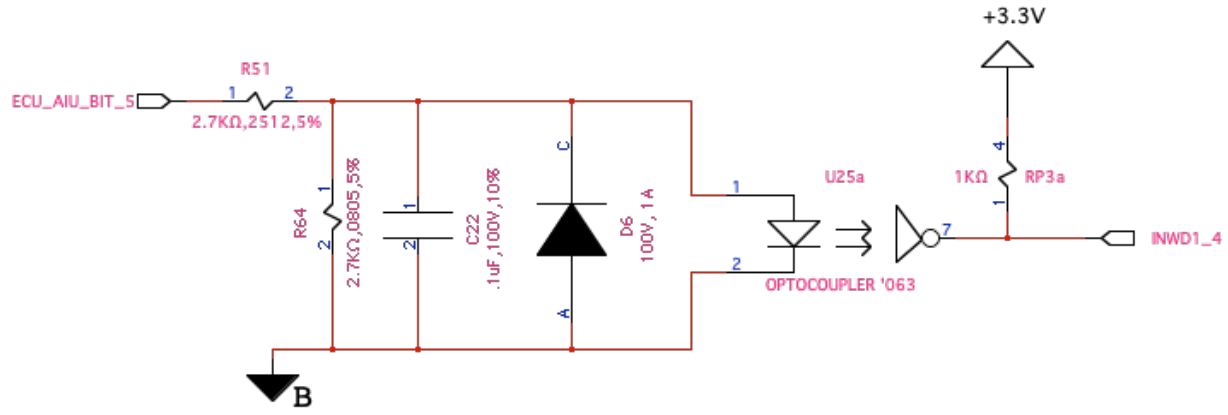


FIGURE 2 BASEBOARD BLOCK DIAGRAM

The Xilinx provides the “brains” for the BaseBoard design. The Host processor mounted to the BaseBoard will task the Xilinx to filter data or look for transitions or load the 429 data etc. The Xilinx has the state-machines and other logic to take the PCI

based commands and to create the proper control and data sequence for the external devices and filtering, interrupt generation etc. for the internal processes.

The OPTOISO inputs are based on circuits similar to the next diagram.



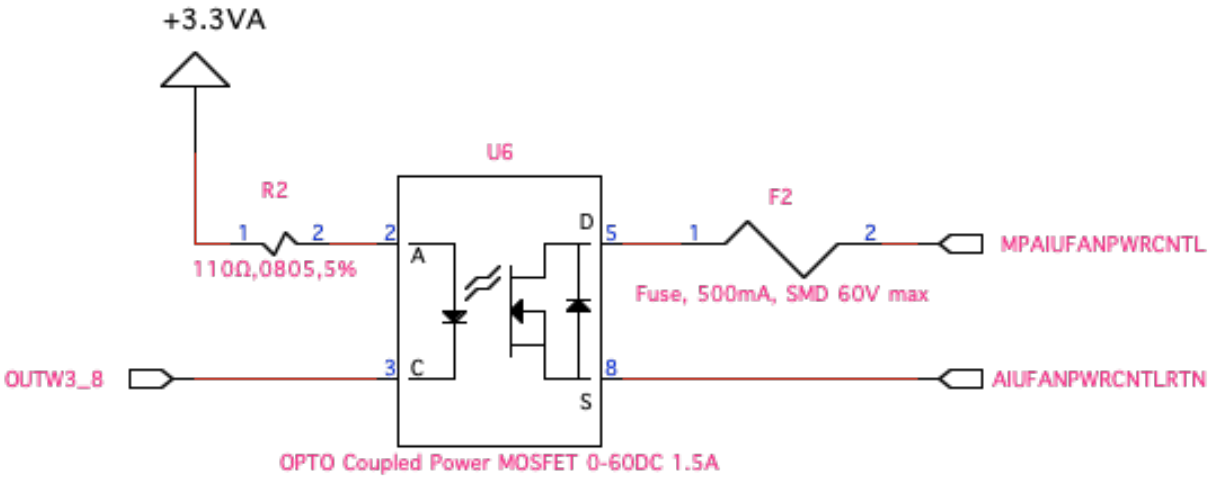
The input signal when “high” will turn on the LED of the optocoupler and drive the received bit to the Xilinx. The optocouplers are all in this basic arrangement but with some variations for the reference input voltage to match the type of input being measured. The receiver inverts the data as it operates as an open-drain device. The Xilinx inverts the input bits to compensate. When the LED is turned on the status bit for the unfiltered data will be ‘1’.

Within the Xilinx the data is sampled at a programmable rate. The input bits are arranged in “words”. Each word has a separate programmable clock. Each bit has a separate control register to program the filter to look for active high, active low, Change of state etc. The circuits are designed to operate in a noisy environment and use hysteresis to help. The filter has a programmable threshold for a “low” and “high” value. The values are compared with an up-down counter to determine if the bit should be declared to be a ‘1’ or a ‘0’. The counter acts as accumulator. The hysteresis comes from staying in the ‘0’ state until the counter is into the ‘1’ state and vice-versa.

The Optocoupled outputs are controlled with registers within the Xilinx. The outputs are also organized as “words”. The register bits are used to control open-drain outputs within the Xilinx. The open-drain IO are used to make sure the optocoupler is completely turned off when not enabled.

When the bit is set the open drain IO is driven low to turn on the optocoupler. With the LED turned on the opto isolated FET is turned on and the output connected. In the next

example the FAN Power Control is tied to the return to make a low side switch for an external FAN.



Some of the switches are configured to be high side and some low side. Some have fuse protection and some have resistor coupling depending on the requirements of the external circuit.

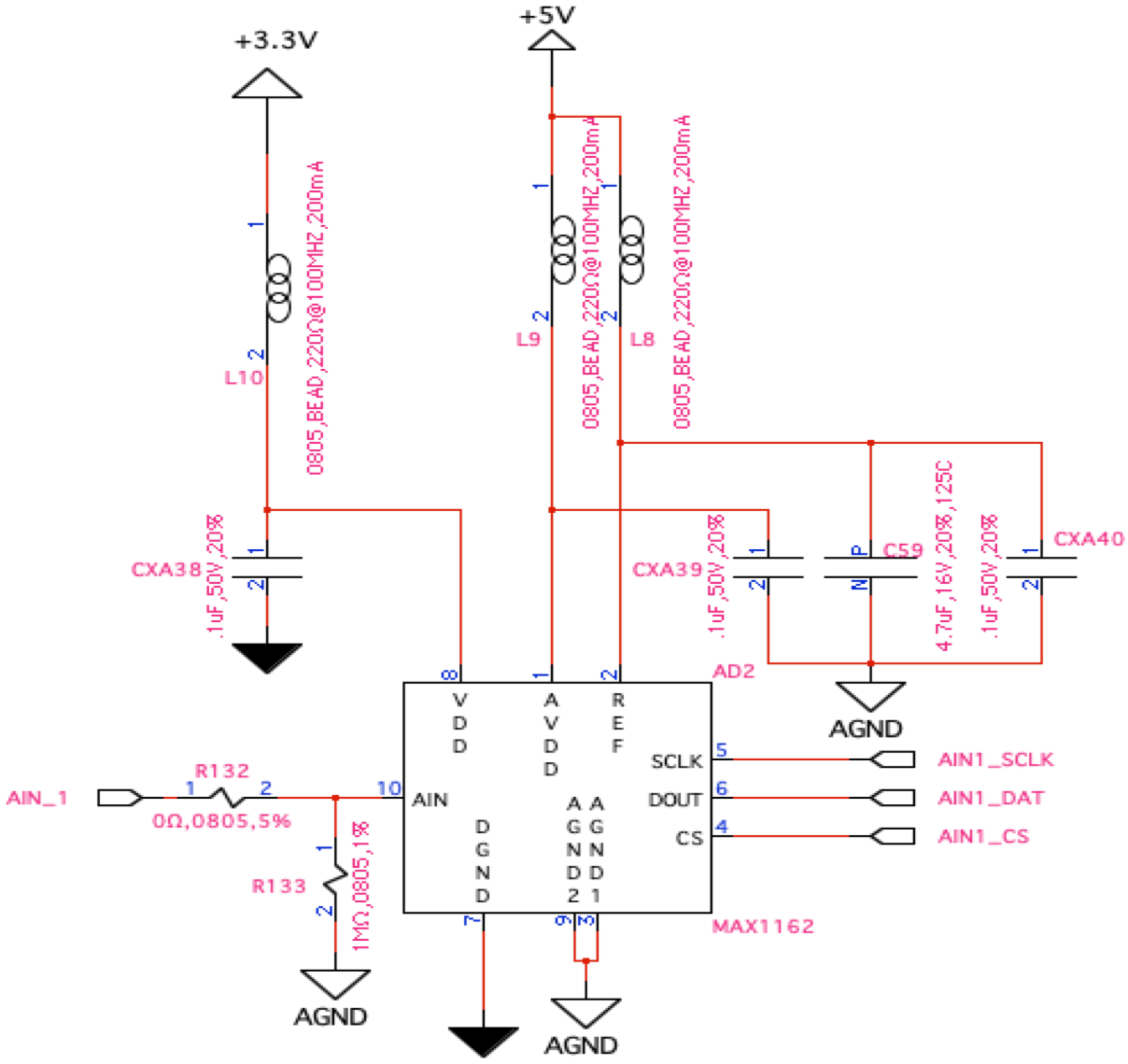
The ARINC 429 interface is made up of two sets of ARINC 429 compatible interface chips. Each set has a controller with a pair of built-in receivers and a separate transmitter buffer. One receiver and one transmitter are connected from each chip set to connectors. The Xilinx is tied to both receiver channels.

The PCI bus is 32 bits and the ARINC devices are 16. The PCI bus is much faster than the local bus to the ARINC chips. The Xilinx takes care of converting 32 bit TX data to 16 bit writes and the timing required to load the devices. The ready bit can be used to determine when the next data can be written. When data is available to read from the device the Xilinx retrieves it and stores it before telling the CPU that data is ready to allow the CPU to retrieve the data in one read without added delays accessing the ARINC devices.

The transorbs required by the ARINC 429 specification are located on a separate interface.

There are 4 A/D and 4 D/A IO provided. Each of the devices is 16 bits and 200 KHz. rated for operation. The devices are separately interfaced to allow individual or parallel

operation depending on the requirements. Each A/D and D/A has power filtering in the form of a filter bead and added capacitors for improved performance. The Analog channels have a voltage divider capability [resistor positions] designed into the BaseBoard to allow for out-of-range voltage measurements.



Typical A/D circuit on BaseBoard.

The Xilinx provides two UART circuits. The UARTs operate in half-duplex mode and have programmable baud, parity, and stop bit capabilities. A pair of RS-485

transceivers convert between the single ended Xilinx signals and the differential external IO standard.

The channels are programmed to come up as receivers and can become transmitters under software control.

The two channels could be combined to make one full-duplex channel should that be required.

Address Map

```
BB_BASE      0x0000 // 0  base control register offset
BB_WD3       0x0004 // 1  Word 3 data output register
BB_WD4       0x0008 // 2  Word 4 data output register
BB_WD5       0x000C // 3  Word 5 data output register
BB_WD1       0x0010 // 4  Word 1 filtered and unfiltered data
BB_WD2       0x0014 // 5  Word 2 filtered and unfiltered data
BB_WD6       0x0018 // 6  Word 6 filtered and unfiltered data
BB_WD1_CLK   0x001C // 7  Word 1 clock control
BB_WD2_CLK   0x0020 // 8  Word 2 clock control
BB_WD6_CLK   0x0024 // 9  Word 6 clock control
BB_WD1_0     0x0028 // 10 Word 1 bit 0 control
BB_WD1_1     0x002C // 11 Word 1 bit 1 control
BB_WD1_2     0x0030 // 12 Word 1 bit 2 control
BB_WD1_3     0x0034 // 13 Word 1 bit 3 control
BB_WD1_4     0x0038 // 14 Word 1 bit 4 control
BB_WD1_5     0x003C // 15 Word 1 bit 5 control
BB_WD1_6     0x0040 // 16 Word 1 bit 6 control
BB_WD1_7     0x0044 // 17 Word 1 bit 7 control
BB_WD1_8     0x0048 // 18 Word 1 bit 8 control
BB_WD1_9     0x004C // 19 Word 1 bit 9 control
BB_WD1_10    0x0050 // 20 Word 1 bit 10 control
BB_WD1_11    0x0054 // 21 Word 1 bit 11 control
BB_WD1_12    0x0058 // 22 Word 1 bit 12 control
BB_WD2_0     0x005C // 23 Word 2 bit 0 control
BB_WD2_1     0x0060 // 24 Word 2 bit 1 control
BB_WD2_2     0x0064 // 25 Word 2 bit 2 control
BB_WD2_3     0x0068 // 26 Word 2 bit 3 control
BB_WD2_4     0x006C // 27 Word 2 bit 4 control
BB_WD2_8     0x0070 // 28 Word 2 bit 8 control
BB_WD2_10    0x0074 // 29 Word 2 bit 10 control
BB_WD2_11    0x0078 // 30 Word 2 bit 11 control
BB_WD2_12    0x007C // 31 Word 2 bit 12 control
BB_WD2_13    0x0080 // 32 Word 2 bit 13 control
BB_WD2_14    0x0084 // 33 Word 2 bit 14 control
BB_WD2_15    0x0088 // 34 Word 2 bit 15 control
BB_WD6_0     0x008C // 35 Word 6 bit 0 control
BB_WD6_1     0x0090 // 36 Word 6 bit 1 control
BB_WD6_2     0x0094 // 37 Word 6 bit 2 control
BB_WD6_3     0x0098 // 38 Word 6 bit 3 control
BB_WD6_4     0x009C // 39 Word 6 bit 4 control
BB_WD6_8     0x00A0 // 40 Word 6 bit 8 control
BB_WD6_9     0x00A4 // 41 Word 6 bit 9 control
```

```
BB_WD6_13          0x00A8 // 42 Word 6 bit 13 control
BB_WD6_14          0x00AC // 43 Word 6 bit 14 control
BB_WD6_15          0x00B0 // 44 Word 6 bit 15 control
BB_WD1_INT         0x00B4 // 45 WD 1 Interrupts
BB_WD2_INT         0x00B8 // 46 WD 2 Interrupts
BB_WD6_INT         0x00BC  // 47 WD 6 Interrupts
BB_LD_TX0_429      0X00C0 // 48 Load TX0 429 Data
BB_LD_TX1_429      0x00C4 // 49 Load TX1 429 Data
BB_LD_CNTL0_429 0x00C8 // 50 Load Control 0 429
BB_LD_CNTL1_429  0x00CC // 51 Load Control 1 429
BB_RX_0_1_429      0x00D0 // 52 Read device 0 channel 1 429
BB_RX_0_2_429      0x00D4 // 53 reserved for device 0 channel 2
BB_RX_1_1_429      0x00D8 // 54 Read device 1 channel 1 429
BB_RX_1_2_429      0x00DC // 55 reserved for device 1 channel 2
BB_429_INT         0x00E0 // 56 429 and UART Interrupts
BB_UART0_CNTL      0x00E4 // 57 Control for UART 0
BB_UART0           0x00E8 // 58 Data port for UART 0
BB_UART1_CNTL      0x00EC // 59 Control for UART 1
BB_UART1           0x00F0 // 60 Data port for UART 1

BB_AN_STAT         0x00FC // 63 Analog status

BB_DAC_0           0x0118 // 70 DAC 0
BB_DAC_1           0x011C // 71 DAC 1
BB_DAC_2           0x0120 // 72 DAC 2
BB_DAC_3           0x0124 // 73 DAC 3
BB_ADC_0           0x0128 // 74 ADC 0
BB_ADC_1           0x012C // 75 ADC 1
BB_ADC_2           0x0130 // 76 ADC 2
BB_ADC_3           0x0134 // 77 ADC 3
```

FIGURE 3 BASEBOARD INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the BaseBoard. The addresses are all offsets from a base address, which is assigned by the system when the PCI bus is configured.

The VendorId = 0x10EE. The CardId = 0x0020. Current revision = 0x00

Programming

Programming the BaseBoard requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the BaseBoard "registration" data. In other systems the discovery is automatic.

In order to receive data, software is only required to enable the Rx FIFO, and Rx state machine for the channels of interest. To transmit, software will need to load the message into the appropriate channel FIFO, set the frequency and enable the transmitter.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the channel interrupts, the COS interrupts or both. After the interrupt is received, the data can be retrieved. An efficient loop can then be implemented to fetch the data. New messages can be received even as the current one is read from the FIFO.

The TX interrupt indicates to the software that a message has been sent and that the message has completed. If more than one interrupt is enabled, then the SW needs to read BB_WD1_INT, BB_WD2_INT, BB_WD6_INT etc. to see which source caused the interrupt. The status bits are latched and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status registers and write that value back to clear all the latched interrupt status bits before starting a process. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

Register Definitions

BB_BASE

[$00] BaseBoard Base Control Register Port read/write

CONTROL BASE

DATA BIT	DESCRIPTION
31-21	Spare
20	test clock select
19-18	Spare
17	ADC Master Enable
16	DAC Master Enable
15	Spare
14	DBCEN_1N
13	RESET_1N
12	ENTX_1
11	Spare
10	DBCEN_0N
9	RESET_0N
8	ENTX_0
7	EN_RX_1_2 [set to ‘0’]
6	EN_RX_1_1
5	EN_RX_0_2 [set to ‘0’]
4	EN_RX_0_1
3	LED_DIS_4
2	LED_DIS_3
1	Interrupt Set
0	Interrupt Enable Master

FIGURE 4 BASEBOARD BASE CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

Interrupt Enable Master when '1' allows interrupts generated by the BaseBoard to be driven onto the backplane [INTA]. When '0' the interrupts can be individually enabled and used for status without driving the backplane. Polled operation can be performed in this mode.

Interrupt Set when '1' and the Master is enabled, forces an interrupt request. This feature is useful for testing and software development.

LED_DIS_3 and LED_DIS_4 are used as master enables/disables for the output words 3 and 4. When cleared ‘0’ the output bits defined in the output word registers will be created with the optocouplers. When ‘1’ the Word 3 and 4 output registers will not affect the optocouplers.

The EN_RX bits are used to enable the ARINC 429 channels associated with the bits. Channel 2 on device 0 and 1 are not currently connected to the IO connector and should remain not enabled. Channel 1 of each device are used for the two channels.

ENTX_0, and ENTX_1 are used to control sending and loading data from the TX channels. When ‘1’ the transmitter is enabled to send data. When ‘0’ the transmitter is held off from sending and loading can take place. This signal should be used in conjunction with the TX ready bits. Once set the bits should remain set until the channel is finished transmitting or data will be lost. See the 429 device interface manual for more information.

RESET_0N, RESET_1N need to be cleared to ‘0’ to clear the 429 devices. To initialize the 429 devices the signals need to be cleared to ‘0’ and held for 200 nS or more then set to ‘1’ for normal operation.

Please note that the reset clears the transmitter memory, bit counters, word counter, gap timers, Drn and TXR. The control register within the Arinc device is not affected.

DBCEN_0N and DBCEN_1N are tied to the bits with the same names on Device 0 and Device 1 [429] . These bits are normally left set to ‘0’. See the 429 Device interface manual for more information.

DAC master enable when ‘1’ allows the local enables to start a Digital to Analog conversion. When ‘’0’ the local enables are held for the master enable to allow multiple channels to be synchronized. Leave as ‘1’ for random access. Switch to ‘0’ to load and ‘1’ to send for synchronized access.

ADC Master Enable when ‘1’ allows the local enable to cause an Analog to Digital conversion cycle to take place. When ‘0’ the local enable is held off. For decoupled operation leave in the ‘1’ state. For synchronized data capture leave in ‘0’ until the channel’s local enables are set then set to ‘1’ for a synchronous conversion across channels.

Test Clock Select when ‘0’ has no affect and is the standard setting. When ‘1’ the Test

Clock Select routes the Word 6 filter reference clock to the UART B data out line. The UART B 485 buffer is located on the front surface and makes an easy access for scope verification of programmed frequencies.

BB_WD3, BB_WD4, BB_WD5

[$04, $08, $0C] BaseBoard Output Word Register Port read/write

Output Word Defintions

DATA BIT	DESCRIPTION
15-0	Output Word Definition

FIGURE 5 BASEBOARD OUTPUT WORD REGISTER BIT MAP

The output "words" are tied to the connectors via opto-couplers. When LED_3 is enabled the bits of BB_WD3 are used to control the optocouplers of word 3 When LED_4 is enabled the bits of BB_WD4 are used to control the optocouplers of word 4. Word 5 is always enabled. The optocouplers are enabled when the corresponding bit is set to '1'. The outputs are open drain and inverted on hardware to control the optocoupler. There are fewer output bits than Output Word definitions. The active bits are those corresponding to the output definitions.

Bit 4 of word 5 is tied to a comparator rather than an opto-coupler. This output is not implemented as open drain. '1' = '1'.

Bit 13 of word 4 corresponds to the warm-up LED and is configured to come up on and be disabled with a '1' in its bit position.

Word 3 has active bits in positions: 0-6,8-11,13,14
Word 4 has active bits in positions: 0-14
Word 5 has active bits in positions: 0-5,8-11

BB_WD1

[$10 BaseBoard Input Word1 Data Port read

Input Word1 Status Port

DATA BIT	DESCRIPTION
31-29	spare
28	INWD1_12
27	INWD1_11
26	INWD1_10
25	INWD1_9
24	INWD1_8
23	INWD1_7
22	INWD1_6
21	INWD1_5
20	INWD1_4
19	INWD1_3
18	INWD1_2
17	INWD1_1
16	INWD1_0
15-13	spare
12	bit_1_12
11	bit_1_11
10	bit_1_10
9	bit_1_9
8	bit_1_8
7	bit_1_7
6	bit_1_6
5	bit_1_5
4	bit_1_4
3	bit_1_3
2	bit_1_2
1	bit_1_1
0	bit_1_0

FIGURE 6 BASEBOARD WORD 1 BIT MAP

The INWD1_X bits are the straight data from the opto-couplers. The data is inverted in hardware to compensate for the inversion created by the opto-coupler receiver devices.

The bit_1_Y bits are the current definitions from the COS detector. The bit_1 values will tend to lag the INWD1 values.

BB_WD2

[$14 BaseBoard Input Word 2 Data Port read

Input Word2 Status Port

DATA BIT	DESCRIPTION
31	INWD2_15
30	INWD2_14
29	INWD2_13
28	INWD2_12
27	INWD2_11
26	INWD2_10
25	spare
24	INWD2_8
23	gnd
22	gnd
21	gnd
20	INWD2_4
19	INWD2_3
18	INWD2_2
17	INWD2_1
16	INWD2_0
15	bit_2_15
14	bit_2_14
13	bit_2_13
12	bit_2_12
11	bit_2_11
10	bit_2_10
9	gnd
8	bit_2_8
7-5	spare
4	bit_2_4
3	bit_2_3
2	bit_2_2
1	bit_2_1
0	bit_2_0

FIGURE 7 BASEBOARD WORD 2 BIT MAP

The INWD2_X bits are the straight data from the opto-couplers. The data is inverted in hardware to compensate for the inversion created by the opto-coupler receiver devices.

The bit_2_Y bits are the current definitions from the COS detector. The bit_2 values will tend to lag the INWD2 values.

BB_WD6

[$18 BaseBoard Input Word 6 Data Port read

Input Word6 Status Port

DATA BIT	DESCRIPTION
31	INWD6_15
30	INWD6_14
29	INWD6_13
28-26	spare
25	INWD6_9
24	INWD6_8
23-21	spare
20	INWD6_4
19	INWD6_3
18	INWD6_2
17	INWD6_1
16	INWD6_0
15	bit_6_15
14	bit_6_14
13	bit_6_13
12-10	spare
9	bit_6_9
8	bit_6_8
7-5	spare
4	bit_6_4
3	bit_6_3
2	bit_6_2
1	bit_6_1
0	bit_6_0

FIGURE 8 BASEBOARD WORD 6 BIT MAP

The INWD6_X bits are the straight data from the opto-couplers. The data is inverted in hardware to compensate for the inversion created by the opto-coupler receiver devices.

The bit_6_Y bits are the current definitions from the COS detector. The bit_6 values will tend to lag the INWD6 values.

BB_WD1_CLK, BB_WD2_CLK, BB_WD6_CLK

[$1C, $20, $24] BaseBoard Clock Control Registers Port read/write

Clock Control RX	
DATA BIT	**DESCRIPTION**
31-21	Spare
20-19	reference select
18	output select
17-0	divisor

FIGURE 9 BASEBOARD TX CONTROL BIT MAP

Reference Select:
when 00 ,01,10 selects the PCI clock = 33 MHz
when 11 the PCI clock pre-scaled [/2] is selected

The reference selected is divided using the selected divisor and then divided in half for a 50% duty cycle reference clock. F = R/2*(D+1). Where F = the frequency desired, R = the selected reference frequency, and D = the specified divisor. For example to create a 3.3 MHz sample frequency from the standard 33 MHz PCI a divide by 10 is needed. The divisor is 0x04. {[2(4+1)] = 10}

The output select when '1' selects the output from the divider. When '0' the selected reference frequency is used.

Each input word has its own programmable reference clock. Please remember to convert to hex when selecting the divisor. For a 1 mS sample rate = 1000 Hz. 33 Mhz/1000 Hz = 33000. N = 16,499 => 0x4073 for the divisor.

BB_Wdx_y

[$28 - $B0] BaseBoard RX Bit Control Register Port read/write

RX BIT CONTROL	
DATA BIT	**DESCRIPTION**
31-21	Spare
20	Clear
19	Enable
18	Invert
17	Falling
16	Rising
15-8	High Threshold
7-0	Low Threshold

FIGURE 10 BASEBOARD RX BIT CONTROL MAPS

Each of the Optocoupled inputs has a filter associated with it. The filter accumulates data and tests the accumulated count against the programmed thresholds to determine the value to assign to the bit. The assigned value has hysteresis. The received bit is cleared to '0' for the accumulated value. The bit is assigned a value of '0' until the count reaches the high threshold. Once assigned a high value the accumulated count must go below the low threshold to switch back to a '0' assigned value.

The counter when enabled counts up for each '1' received from sampling the incoming signal with a flip-flop at the programmed rate [see word 1 clock select etc.] The counter decrements for each '0' received. The counter holds at a value if "00" or "FF" and trying to decrement or increment respectively to prevent over-flow and under-flow conditions from changing the assigned value. If the counter is disabled and then re-enabled the count will restart from that value and the assigned output value will stay constant.

If the Clear is set '1' the counter is forced to "00" and the assigned value will return to '0'.

The invert bit will invert the sampled data coming into the accumulator. There is a mux after the initial sampling logic which selects the straight or inverted data to be presented to the accumulator. '0' is normal. '1' is inverted data.

Rising when set '1' will cause the Change of State detector to capture a change in assigned value from 0 => 1. Falling when set '1' will capture the 1 => 0 transition. Either, neither or both can be set. The COS detector will create a pulse to the interrupt generation logic. The Rising and Falling bits act as interrupt enables for those

conditions on the bit the register is tied to. All bits and edges are independent. The status can be read from the INT registers assigned to each word.

BB_WD1_INT

[$B4] BaseBoard Input Word1 Interrupt Status read/write

Input Word1 Interrupt Status

DATA BIT	DESCRIPTION
31-26	Spare
25	COS Falling Bit 12
24	COS Rising Bit 12
23	COS Falling Bit 11
22	COS Rising Bit 11
21	COS Falling Bit 10
20	COS Rising Bit 10
19	COS Falling Bit 9
18	COS Rising Bit 9
17	COS Falling Bit 8
16	COS Rising Bit 8
15	COS Falling Bit 7
14	COS Rising Bit 7
13	COS Falling Bit 6
12	COS Rising Bit 6
11	COS Falling Bit 5
10	COS Rising Bit 5
9	COS Falling Bit 4
8	COS Rising Bit 4
7	COS Falling Bit 3
6	COS Rising Bit 3
5	COS Falling Bit 2
4	COS Rising Bit 2
3	COS Falling Bit 1
2	COS Rising Bit 1
1	COS Falling Bit 0
0	COS Rising Bit 0

FIGURE 11 BASEBOARD INTERRUPT WORD1 BIT MAP

Each bit in word 1 has the potential for two interrupt status bits. The Rising and the Falling bits are generated in response to the Change of State detector and enabled by the Rising and Falling control bits. The bits when set will cause an interrupt to the CPU assuming that the master interrupt enable is active. The interrupts are latched and held

until explicitly cleared by writing a '1' to the same bit location or locations. It is not necessary to write a '0' to re-enable after the clear. Clearing the interrupts as part of the initialization process or whenever the parameters [Rising and Falling] are changed [to make sure the change in set-up is not interpreted as a change in status] is recommended. If the master enable is disabled the bits can be used in a polled mode.

BB_WD2_INT

[$B8] BaseBoard Input Word2 Interrupt Status read/write

Input Word2 Interrupt Status

DATA BIT	DESCRIPTION
31	COS Falling Bit 15
30	COS Rising Bit 15
29	COS Falling Bit 14
28	COS Rising Bit 14
27	COS Falling Bit 13
26	COS Rising Bit 13
25	COS Falling Bit 12
24	COS Rising Bit 12
23	COS Falling Bit 11
22	COS Rising Bit 11
21	COS Falling Bit 10
20	COS Rising Bit 10
19-18	spare
17	COS Falling Bit 8
16	COS Rising Bit 8
15-10	spare
9	COS Falling Bit 4
8	COS Rising Bit 4
7	COS Falling Bit 3
6	COS Rising Bit 3
5	COS Falling Bit 2
4	COS Rising Bit 2
3	COS Falling Bit 1
2	COS Rising Bit 1
1	COS Falling Bit 0
0	COS Rising Bit 0

FIGURE 12 BASEBOARD INTERRUPT WORD2 BIT MAP

Each bit in word 2 has the potential for two interrupt status bits. The Rising and the Falling bits are generated in response to the Change of State detector and enabled by

the Rising and Falling control bits. The bits when set will cause an interrupt to the CPU assuming that the master interrupt enable is active. The interrupts are latched and held until explicitly cleared by writing a '1' to the same bit location or locations. It is not necessary to write a '0' to re-enable after the clear. Clearing the interrupts as part of the initialization process or whenever the parameters [Rising and Falling] are changed [to make sure the change in set-up is not interpreted as a change in status] is recommended. If the master enable is disabled the bits can be used in a polled mode. The status bits are arranged to match their natural order.

BB_WD6_INT

[$BC] BaseBoard Input Word6 Interrupt Status read/write

Input Word6 Interrupt Status

DATA BIT	DESCRIPTION
31	COS Falling Bit 15
30	COS Rising Bit 15
29	COS Falling Bit 14
28	COS Rising Bit 14
27	COS Falling Bit 13
26	COS Rising Bit 13
25-20	spare
19	COS Falling Bit 9
18	COS Rising Bit 9
17	COS Falling Bit 8
16	COS Rising Bit 8
15-10	spare
9	COS Falling Bit 4
8	COS Rising Bit 4
7	COS Falling Bit 3
6	COS Rising Bit 3
5	COS Falling Bit 2
4	COS Rising Bit 2
3	COS Falling Bit 1
2	COS Rising Bit 1
1	COS Falling Bit 0
0	COS Rising Bit 0

FIGURE 13 BASEBOARD INTERRUPT WORD6 BIT MAP

Each bit in word 6 has the potential for two interrupt status bits. The Rising and the

Falling bits are generated in response to the Change of State detector and enabled by the Rising and Falling control bits. The bits when set will cause an interrupt to the CPU assuming that the master interrupt enable is active. The interrupts are latched and held until explicitly cleared by writing a '1' to the same bit location or locations. It is not necessary to write a '0' to re-enable after the clear. Clearing the interrupts as part of the initialization process or whenever the parameters [Rising and Falling] are changed [to make sure the change in set-up is not interpreted as a change in status] is recommended. If the master enable is disabled the bits can be used in a polled mode. The status bits are arranged to match their natural order.

429 Ports

```
BB_LD_TX0_429      0X00C0 // 48 Load TX0 429 Data
BB_LD_TX1_429      0x00C4 // 49 Load TX1 429 Data
BB_LD_CNTL0_429 0x00C8 // 50 Load Control 0 429
BB_LD_CNTL1_429  0x00CC // 51 Load Control 1 429
BB_RX_0_1_429      0x00D0 // 52 Read device 0 channel 1 429
BB_RX_0_2_429      0x00D4 // 53 reserved for device 0 channel 2
BB_RX_1_1_429      0x00D8 // 54 Read device 1 channel 1 429
BB_RX_1_2_429      0x00DC // 55 reserved for device 1 channel 2
BB_429_INT         0x00E0 // 56 429 and UART Interrupts
```

The ARINC 429 interface is accomplished with the Xilinx working in conjunction with the 429 transceiver chip set. The transceiver has a transmit port, two receive ports, and a control port. There are two transceivers on the Baseboard. The transceiver is a 16 bit device. The Xilinx takes care of moving 32 bit data to the transceiver and creating 32 bit data for the host to read back.

The data is directly mapped to the ARINC transceiver. The transceiver re-organizes the bit stream to match the 429 specification. Please refer to page 7 of the 3282 manual for the bit definitions.

When data is written to the BB_LD_Txx_429 ports the data is latched as a 32 bit word. The data is written to the 429 device indicated by the port accessed [0 or 1]. The ready/busy bit is set when the state-machine can handle another command. The data can only be loaded into the transmitter of the 429 device when the ENTX bit for that channel is in the load state [‘0’]. When loading is complete setting ENTX to ‘1’ will cause the data to be sent. The 429 device can store up to 8 words to transmit. When the stored words are transmitted the 429 device asserts the transmitter complete signal which the Xilinx turns into an interrupt request.

When data is available to be read, and the receiver is enabled [En_RX], the tranceiver asserts the DR signal for that channel. The state-machine within the Xilinx responds to the DR signal by reading the data and storing into separate channel registers. The state-machine then notifies the host that the data is ready with an interrupt / status. The tranceivers support two receiver channels each. The transceivers are connected to the Xilinx to support both receive channels per transceiver. *Only one receiver per device is connected to an IO connector at this time*. The second receiver can be activated if that is required. The VHDL would be updated to allow the second channel to be enabled and two connections made between the transceiver and a connector.

The Control word ports are used to set-up the 429 device. The bits are mapped to the lower half of the data word [15-0] and should be written as a long word – 0x0000control data. The control word can alter the parity, word length, data rate, etc. The following is copied from the device manual. Updates in BLUE are our comments. Please refer to the '3282 manual for more information. The manual is available for download on the Dynamic Engineering website at the bottom of the IP-429 page.
http://www.dyneng.com/ip429.html

3282 Control Bit Description
15 (MSB) WLSEL
14 RCYSEL
13 TXSEL
12 PARCK
11 Y2
10 X2
09 SDEN2
08 Y1
07 X1
06 SDEN1
05 SLFTST
04 PAREN
03 NOT USED
02 NOT USED
01 NOT USED
00 NOT USED

DBCEN Data bit control enable (input, active Low with internal pull up to Vcc). Logic 0 enables the transmitter parity bit control function as defined by control register bit 4, PAREN. Logic 1 forces transmitter parity bit insertion regardless of PAREN value. Pin is normally left open or tied to GND.
Normally programmed '0' in BB_Base.

PAREN Transmitter Parity Enable (Bit 4). Enables parity bit insertion into transmitter data bit 32. Parity is always inserted if DBCEN (Pin 40) is open or HI. If DBCEN is LO, Logic 0 on PAREN inserts data on bit 32, and Logic 1 on PAREN inserts parity on bit 32.
For operation parity is inserted['1'], for external loop-back testing parity is not inserted['0'].

SLFTST Å Self Test Enable (Bit 5). Logic 0 enables a wrap–around test mode which internally connects the transmitter outputs to both receiver inputs, bypassing the receiver front end. The test data is inverted before going into Receiver 2, so its data is the complement of that received by Receiver 1. The transmitter output is active during test mode.
Normally programmed ‘0

SDEN1 Ç S/D Code Check Enable RX1 (Bit 6). Logic 1 enables the Source/Destination Decoder for Receiver 1. X1,Y1 Ç S/D Compare Code RX1 (Bit 7, Bit 8). If the Receiver 1 S/D code check is enabled (SDENB1 = 1), then incoming receiver data S/D fields will be compared to Xl,Yl. If they match, the word will be accepted by Receiver 1; if not, it will be ignored. X1 (Bit 7) is compared to serial data bit 9, Y1 (Bit 8) is compared to serial data bit 10.

SDEN2 Ç S/D Code Check Enable RX2 (Bit 9). Logic 1 enables the Source/Destination Decoder for Receiver 2. X2,Y2 Ç S/D Compare Code RX2 (Bit 10, Bit 11). If the Receiver 2 S/D code check is enabled (SDENB2 = 1), then incoming receiver data S/D fields will be compared to X2,Y2. If they match, the word will be accepted by Receiver 2; if not, it will be ignored. X2 (Bit 10) is compared to serial data bit 9, Y2 (Bit 11) is compared to serial data bit 10.

The SDEN1/2 and X1,Y1/X2,Y2 bits are frequently not needed [set to ‘0’]. Some data filtering can be achieved with these bits. Additional filtering or perhaps enhanced filtering can be added by updating the VHDL code to only interrupt / save certain labels on the 429 data. This feature is not currently implemented.

PARCK Parity Check Enable (Bit 12). Logic 1 inverts the transmitter parity bit. Logic 0 selects normal odd parity; logic 1 selects even parity.

TXSELÉ Transmitter Data Rate Select (Bit 13). Logic 0 sets the transmitter to the HI data rate. HI rate is equal to the clock rate divided by 10 (100 kbps for 1 MHz clock). Logic 1 sets the transmitter to the LO data rate. LO rate is equal to the clock rate divided by 80 (12.5 kbps for 1 MHz clock). RCVSELÑ Receiver Data Rate Select (Bit 14). Logic 0 sets both receivers to accept the HI data rate. The nominal HI data rate is the input clock divided by 10 (100 kbps for 1 MHz clock). Logic 1 sets both receivers to accept the LO data rate. The nominal LO data rate is the input clock divided by 80 (12.5 kbps for 1 MHz clock).
The clock rate is dependent on the system architechture – what devices are attached to the ‘429 bus. There are two separate 429 transceivers available to allow for 1 high and 1 low or two of the same frequency.

WLSELÖ Word Length Select (Bit 15). Logic 0 sets the transmitter and receivers to a

32-bit word format. Logic 1 sets them to a 25-bit word format.

NOT USED – set to ‘0’.

NOTES: Å The test mode should always conclude with ten nulls. This step prevents both receivers from accepting any invalid data stream. Ç SDENBn, Xn and Yn should be changed within 20 bit times after DRn goes low and after the bit stream has been read, or within 30-bit times after a master reset has been removed. É TXSEL should only be changed during the time that TXR is high or Master Reset is low. Ñ RCVSEL should be changed only during a Master Reset pulse. If changed at any other time, then the next bit stream from both Receiver 1 and Receiver 2 should be ignored. Ö If the control word (which includes WLSEL) is set during Master Reset, the Receiver/Transmitter operation will be correct. If the control word is changed other than during Master Reset, then TXR must be TRUE to ensure correct operation of the transmitter, and the first data stream received, in each receiver, should be ignored.

BB_429_INT

$E0

BIT	Definition
0	rx_0_1_rdy
1	rx_0_2_rdy
2	rx_1_1_rdy
3	rx_1_2_rdy
4	tx_0_rdy
5	tx_1_rdy
6	gnd
7	gnd
8	uarta_dn
9	uarta_dav
10	uarta_frm
11	uarta_par
12	uartb_dn
13	uartb_dav
14	uartb_frm
15	uartb_par
16	ready_busy_429
17	tx_0_stat
18	tx_1_stat
31-19	gnd

FIGURE 14 BASEBOARD 429 AND UART STATUS REGISTER

Bits remain set until explicitly cleared by writing to this port with the corresponding bit set. It is recommended that the bits are tested and cleared [or just cleared] before starting a new operation with the 429 or UART. For example if you set up the UART then clear any pending status after the set-up before enabling interrupts to make sure that a stored condition is not treated as a new condition.

RX_0_1_RDY when '1' indicates that data is ready to be ready from the device 0 channel 1 port.

RX_0_2_RDY when '1' indicates that data is ready to be ready from the device 0 channel 2 port. This port is currently inactive.

RX_1_1_RDY when '1' indicates that data is ready to be ready from the device 1 channel 1 port.

RX_1_2_RDY when '1' indicates that data is ready to be ready from the device 1

channel 2 port. This port is currently inactive.

TX_0_RDY when ‘1’ indicates that the data written to the device 0 transmitter port and enabled has been sent.

TX_1_RDY when ‘1’ indicates that the data written to the device 1 transmitter port and enabled has been sent.

Ready_Busy_429 when ‘1’ indicates that the state-machine is ready for another command. When ‘0’ the state-machine is processing a command. The two devices have individual storage registers or Transmit, Command and Receive words. You can overlap writes to the two channels or different types of registers [with care]. When writing to the same channel repeatedly, wait for Ready_Busy to become Ready before writing again.

CMD0 CMD1 TX0 TX1 [wait for ready = 1] TX0 TX1 [wait for ready = ‘1’ etc.

When receive data is available the state-machine will automatically read and store it. The state-machine will be “busy” during this time.

TX_0_STAT, TX_1_STAT are synchronized inputs based on the TXR signal from the 429 device. When ‘1’ the device buffer is empty and ready to accept new data. Please note that this signal is not captured and held or cleared like the other bits in this register.

UARTA_DN, UARTB_DN when ‘1’ indicate that a transmission has completed on the UART. Please note that the direction control must be set to transmit. This bit only has meaning when in transmit mode and should be masked when receiving.

UARTA_DAV, UARTB_DAV when ‘1’ indicate that data is available to read from the data port. Please note that the direction control must be set to receive. This bit only has meaning when in receive mode and should be masked when transmitting.

UARTA_FRM, UARTB_FRM when ‘1’ indicates that a framing error has been detected. This bit only has meaning when in receive mode and should be masked when transmitting.

UARTA_PAR, UARTB_PAR when ‘1’ indicates that a parity error has been detected. Parity sense is controlled in the UART control register. This bit only has meaning when in receive mode and should be masked when transmitting.

BB_UART0_CNTL,BB_UART1_CNTL

[$E4,$EC] BaseBoard UART control read/write

UART Control Register Bit Map

DATA BIT	DESCRIPTION
31-16	spare
15	Direction: 0 = receive, 1 = transmit
14-13	spare
12-4	Divisor Setting
3	1 = use 2 stop bits, 0 = use 1 stop bit
2	1 = use odd parity
1	1 = parity enable
0	1 = enable UART

FIGURE 15 BASEBOARD UART CONTROL BIT MAP

UARTA and UARTB [alternatively called UART0 and UART1 respectively] are controlled by these ports. The baud rate, Parity, stop bits, enable and direction affect both the TX and RX capabilities of each UART.

Enable when ‘1’ enables the UART to transmit and to receive characters. The UART will automatically transmit when a character is loaded into the holding register.

Parity enable when ‘1’ causes parity to be inserted into the data stream and for parity to be checked on the incoming signal.

Parity when ‘1’ selects odd parity and when ‘0’ even parity. Note that parity enable must be ‘1’ for this bit to be applied to the data.

Stop when ‘0’ puts 1 stop bit at the end of the character sent. Stop when ‘1’ puts 2 stop bits at the end of the message. If there is more data to send the stop bit(s) is/are immediately followed by the next start bit. If there is no more data to send then marking bits are sent until there is data to send.

Direction when ‘1’ enables the 485 transceiver to transmit data from the UART When ‘0’ the transceiver is in the receiver direction. Because of reset circuitry the device will default to receive.

For full duplex operation use both channels together – one for TX and one for Receive. Both sides of the UART [TX and RX] are controlled with the same enable bit per

channel. When enabled the Transmitter will transmit based on data written to the character register and the Receiver will capture data on the lines.

The status from the receiver should be ignored when transmitting. When the external transceiver is set to transmit the receiver side may detect framing and other errors due to the direction of the transceiver. When operating in half duplex mode it is important to clear any receive errors after switching directions to receive.

The BAUD rate is 18.432MHz/ [16 * Divisor]

BB_UART0,BB_UART1

[$E8,$F0] BaseBoard UART control read/write

UART DATA Register

DATA BIT	DESCRIPTION
31-8	spare
7-0	UART Data

FIGURE 16 BASEBOARD UART BIT MAP

After setting up the UART for direction, parity, etc. using the BB_UARTx_CNTL register one can communicate with the UART via the BB_UARTx port. Transmitting will happen automatically by writing to the port. When the DAV status is true received data can be read from the port. The port is read / write in the sense that data is written to for transmit and read from for receive. The port is not read-write for loop-back purposes.

For BIT it is suggested that the two ports are interconnected at the IO connector. One port set to receive and one to transmit. Write data to the TX port and read back from the RX port, reverse the direction and repeat.

BB_AN_STAT

[$FC] BaseBoard UART control read/write

Analog Status Register

DATA BIT	DESCRIPTION
31-6	spare
15	DAC 3 busy = 1, ready = 0
14	DAC 2 busy = 1, ready = 0
13	DAC 1 busy = 1, ready = 0
12	DAC 0 busy = 1, ready = 0
11-4	spare
3	ADC 3 busy = 1, ready = 0
2	ADC 2 busy = 1, ready = 0
1	ADC 1 busy = 1, ready = 0
0	ADC 0 busy = 1, ready = 0

FIGURE 17 BASEBOARD ANALOG STATUS BIT MAP

The BB_AN_STAT register provides a ready-busy indication of the ADC and DAC ports.

When data is written to the BB_DACx port, the data is converted to a serial data stream and sent to the DAC. During the transfer the port is marked “Busy”. After the transfer is completed the port is marked “ready”.

The DAC has a settling time requirement which is longer than the 16 uS [approximate] that the transfer process takes. Additional time should be added based on the accuracy required.

The ADC port starts operation when the BB_ADCx port is written to. The ADC begins the conversion when the CS line is taken low and requires 8 clocks to convert plus 16 clocks to transfer the data for a total of 24 uS. The Ready line indicates that the data is available to read.

BB_DACx

[0x118,11C,120,124]
The BaseBoard has 4 DAC ports. Each port has a 16 bit data interface. Writing to the data interface automatically triggers the DAC conversion. Each port has a separate storage register and state-machine. With the Master DAC Enable in the Base Register the ports can be coordinated to send new data at the same time or to work independently. The interface with the DAC is serial. The reference clock is 1 Mhz. It takes 16 uS plus synchronization from load to DAC programmed to the new value assuming the Master Enable is in the enabled state.

BB_ADCx

[0x128,12C,130,134]
The BaseBoard has 4 ADC ports. Each port has a 16 bit data interface. Writing to the data interface automatically triggers the ADC conversion. Each port has a separate storage register and state-machine. With the Master ADC Enable in the Base Register the ports can be coordinated to capture new data at the same time or to work independently. The interface with the ADC is serial. The reference clock is 1 Mhz. It takes 24 uS plus synchronization from load to ADC data read assuming the Master Enable is in the enabled state. The ADC requires 8 clocks to do the conversion and 16 to transfer the data.

Interrupts

BaseBoard interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with a BaseBoard interrupt the software must read the status registers to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

For example, the BaseBoard COS detectors generate an interrupt request when a ttrasnition is detected and the Rising - Falling int enables and Master interrupt enable bits are set.

The interrupt is mapped to INTA on the PC/104p connector, which is mapped to a system interrupt when the PCI bus configures. The source of the interrupt is obtained by reading BB_WDn_INT [for COS interrupts]. The status remains valid until that bit in the status register is explicitly cleared.

When an interrupt occurs, the Master interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the latched bit and set the Master interrupt enable bit high again.

Operating in polled mode can be done by monitoring the INT registers. The conditions of interest can be enabled, but the Master interrupt enable left disabled. Then the interrupt status bits can be monitored. If one of the enabled conditions occurs, the interrupt status bit will be set, but unless the Master interrupt enable is set, a system interrupt will not occur.

Word ⇔ Connector Definitions

Pin assignments for Word 1

Bit	Name	Connector location
0	ECU_AIU_BIT_1	P1-51
1	ECU_AIU_BIT_2	P1-35
2	ECU_AIU_BIT_3	P1-18
3	ECU_AIU_BIT_4	P1-34
4	ECU_AIU_BIT_5	P1-17
5	ECU_AIU_BIT_6	P1-33
6	ECU_AIU_BIT_7	P1-50
7	ECU_AIU_BIT_8	P1-16
8	ECU_AIU_BIT_9	P1-32
9	ECU_AIU_EN_CUE	P1-31
10	ECU_AIU_WARM_UP	P1-30
11	ECU_AIU_SNS_FAIL	P1-14
12	ECU_AIU_CM_ACT	P1-49

FIGURE 18 BASEBOARD WORD1 CONNECTOR DEFINITION

Word 1 has 13 opto coupled receivers each with active high configuration. Bits 0-8 are referenced to ECU Discrete RTN. Bits 9-12 are referenced to 28V Filter Ground.

Pin assignments for Word 2

Bit	Name	Connector location
0	FDCP_AIU_GND_RST	P1-2
1	FDCP_AIU_GND_EN	J1-46
2	FDCP_AIU_PWR_CNT	P1-21
3	FDCP_AIU_SLP_CNT	P1-37
4	FDCP_MISSLE_RST	P1-1
8	AIU_BIT_CMD	P2-15
10	OUTW3_6_BUF	INTERNAL FEEDBACK
11	OUTW3_1_BUF	INTERNAL FEEDBACK
12	OUTW3_5_BUF	INTERNAL FEEDBACK
13	OUTW3_4_BUF	INTERNAL FEEDBACK
14	OUTW3_3_BUF	INTERNAL FEEDBACK
15	OUTW3_0_BUF	INTERNAL FEEDBACK

FIGURE 19 BASEBOARD WORD2 CONNECTOR DEFINITION

Word 2 has 11 opto coupled receivers. BIT 11 has an active low configuration, the rest have active high configurations. Bits 0-4 are referenced to FDCP Discrete Common. Bits 8, 10, 12-15 are referenced to 28V Filter Ground. Bit 11 is referenced to 28V Filter out.

Pin assignments for Word 3

Bit	Name	Connector location
0	MPAIUECU_PWR_CNT	P1-11
1	AIU_ECU_SLEEP_EN	P1-48
2	AIU_ECU_IBIT_CMD	P1-28
3	MPAIUJHCUPWR_CNT	P1-41
4	MPAIUHPMBPWR_CNT	P1-44
5	MPAIUPTH_PWR_CNT	P1-42
6	AIU_AC_EGN_EVENT	J1-12
8a	MPAIUFANPWRCNTL	P1-29
8b	AIUFANPWRCNTLRTN	P1-6
9a	MPAIUECSPWRCNTL	P1-10
9b	AIUECSPWRCNTLRTN	P1-38
10	MP_AIU_POD_WOW	P1-46
11	MP_AIU_POD_SLEEP	P1-47
13	MP_AIU_POD_SP_2	P1-45
14	MP_AIU_POD_SP_3	P1-27

FIGURE 20 BASEBOARD WORD3 CONNECTOR DEFINITION

Word 3 has 13 opto-coupled outputs. Bits 0, 3, 4, 5, and 6 are high side switching 28V Filter out. Bits 1, 2, 10,11,13,14 are low side, switching 28V Filter Ground. Bits 8,9 have both sides tied to the connector and can be externally configured to be high or low side.

Pin assignments for Word 4

Bit	Name	Connector location
0	PNL_ECU_STAT_IND	P2-11
1	PNL_AIU_EOM_1_IN	P2-13
2	PNL_AIU_EOM_2_IN	P2-25
3	PNL_AIU_EOM_3_IN	P2-12
4	PNL_AIU_EOM_4_IN	P2-24
5	PNL_AIU_JHCU_IND	P2-23
6	PNL_AIU_LTU_IND	P2-21
7	PNL_AIU_LCU_IND	P2-9
8	PNL_AIU_PTH_IND	P2-10
9	PNL_ECU_WRMUP_IN	P2-22
10	PNL_AIU_SYS_FAIL	P2-8
11	PNL_IBIT_IN_PROG	P2-20
12	PNL_AIU_FAIL_IND	P2-7
13	PNL_WARM_UP_IND	P2-19
14	PNL_POD_STAT_IND	P2-6

FIGURE 21 BASEBOARD WORD4 CONNECTOR DEFINITION

Word 4 has 15 opto-coupled outputs. All bits are low side, switching 28V Filter Ground.

Pin assignments for Word 5

Bit	Name	Connector location
0	28V_A1	J1-5
1	28V_A2	J1-24
2	28V_B1	J1-4
3	28V_B2	J1-23
4	OUTW5_4	Internal comparator drive
5	SW_28V	Internal Enable for 28V to A/B
8s	FDCP_IND_COMMON	J1-14
8d	MPAIUFDCPMIS_IND	J1-32
9	MPAIUFDCPWRM_IND	J1-15
10	MPAIUFDCPFAILIND	J1-31
11	MPAIUFDCPGNDNOT	J1-49

FIGURE 22 BASEBOARD WORD5 CONNECTOR DEFINITION

Word 5 has 10 opto-couplers plus 3 comparators. The first 4 opto-couplers enable the 28V Filter Out power onto the A1, A2, B1 and B2 lines. For safety the 28V is controlled

by two more opto-couplers working in series. The master [SW_28V] must be enabled and the output of the comparators must also be enabled for the 28V to reach the A/B switches.

Bit 8 controls FDCP_IND_COMMON which is tied to MPAIUFDCPMIS_IND when the switch is enabled. The FDCP_IND_COMMON is both connected to P2 and the remaining three opto-couplers. Bit 9 switches the FDCP_IND_COMMON onto the MPAIUFDCPWRM_IND when enabled. Bit 10 switches the FDCP_IND_COMMON onto the MPAIUFDCPFAILIND when enabled. Bit 11 switches the FDCP_IND_COMMON onto the MPAIUFDCPGNDNOT when enabled.

Pin assignments for Word 6

Bit	Name	Connector location
0a	AC_LSI_1_HI	J1-51
0c	AC_LSI_1_LO	J1-35
1a	AC_LSI_2_HI	J1-18
1c	AC_LSI_2_LO	J1-34
2a	AC_LSI_3_HI	J1-17
2c	AC_LSI_3_LO	J1-33
3a	AC_LSI_4_HI	J1-50
3c	AC_LSI_4_LO	J1-16
4	INWD6_4	J1-6
8	INWD6_8	J1-41
9	INWD6_9	J1-7
13	POD_AIU_0V_UN_T	P1-25
14	POD_AIU_UN_RANGE	P1-4
15	POD_AIU_0V_RANGE	P1-5

FIGURE 23 BASEBOARD WORD6 CONNECTOR DEFINITION

Word 6 has 7 opto-coupled inputs plus 3 direct coupled inputs. The bits marked with an A and a B side have both sides tied to the connector. The A side is the ANODE side of the opto-coupler and the C side is the Cathode side. The remaining coupled bits are tied to the cathode side to provide a low side enable to the opto-coupler. The reference is the “28V circuit breaker” power. The direct coupled inputs are expected to be opto-coupled externally. The bits are inverted within the Xilinx to match the other opto-coupled [on the baseboard] bits.

Pin assignments for UART, ADC, DAC, 429

Name	Description	Connector location
422_A+	UART channel A	J2-12
422_A-		J2-13
422_B+	UART channel B	J2-23
422_B-		J2-24
429_0_RX+	ARINC 429 channel	J2-15
429_0_RX-	0 Receive pair	J2-16
429_0_TX+	ARINC 429 channel	J2-1
429_0_TX-	0 Transmit pair	J2-2
429_1_RX+	ARINC 429 channel	J2-8
429_1_RX-	1 Receive pair	J2-9
429_1_TX+	ARINC 429 channel	J2-5
429_1_TX-	1 Transmit pair	J2-6
AIN_0	ADC channel 0	J3-1
AIN_1	ADC channel 1	J3-2
AIN_2	ADC channel 2	J3-3
AIN_3	ADC channel 2	J3-4
AOUT_0	DAC channel 0	J3-5
AOUT_1	DAC channel 1	J3-6
AOUT_2	DAC channel 2	J3-7
AOUT_3	DAC channel 3	J3-8

FIGURE 24 BASEBOARD UART, 429, ADC, DAC CONNECTOR DEFINITION

Pin assignments for Power, GND

Name	Connector location
28V FILTER GND	J1-13,36,19
	P1-39,23,40,24,7,8,9
LOGIC GND	J1-40,25,26
ECU DISCRETE RTN	P1-12,13.15
CHASSIS GND	J2-14,3,18,21,11,25
FDCP DISCRETE COM	J1-30
AIO GND	J3-9,10,11,12,13,14,15
28V FILTER	J1-2,3,21,22
	P2-16,4,17,5
28V CIRCUIT BREAKER	J1-1,20

FIGURE 25 BASEBOARD POWER & GND CONNECTOR DEFINITION

Please note: Rev A boards had 28V filter Ground on P1-21. AIO GND is selectable with resistors to be referenced to Analog or Digital ground.
The PC/104 ISA and PCI power and ground references are not shown.

Applications Guide

Interfacing

The pin-out tables are displayed sorted signal. WDM micro D style connectors are used for the IO. Standard PC/104 connectors are used for the ISA and PCI connectors.
J1 = MWDM1L-51PBSP .110
J2 = MWDM1L-25PBSP .110
J3 = MWDM1L-15PBSP .110
P1 = MWDM1L-51SBSP .110
P2 = MWDM1L-25SBSP .110

The mating connectors are available from GlenAir

Please note that the ISA connectors are only used for power distribution on the BaseBoard. ISA connections within the stack will work, but signals are not interconnected between the stacks.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the BaseBoard when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time.

The BaseBoard design is robust with optocoupler circuits protected with DIODEs and fuses, high wattage IO resistors [2512] etc. OptoIsolated IO are routed with 20 mil traces on 2 oz copper.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the devices rated voltages.

Construction and Reliability

PC/104 Modules were conceived and engineered for rugged industrial environments. BaseBoard is constructed out of 0.062 inch thick hight temp, FR4 material. 2 oz and 1/2 oz copper layers are used to interconnect the BaseBoard. The power planes and optocoupled IO are on 2 oz planes. The FPGA interconnect is 1/2 oz and the outside layers are 1/2 oz.

Through hole and surface mounting of components are used.

The PC/104 module is secured against the BaseBoard with four screws attached to the stand-offs. BaseBoard has a series of mounting holes [20] around the perimeter. The chassis ground plane is exposed around the perimeter to allow good thermal bonding to the chassis for limited air flow environments.

Thermal Considerations

The BaseBoard design consists of CMOS circuits and OptoCoupled FETs. The power dissipation due to internal circuitry is low. It is possible to create a higher power dissipation with the externally connected logic. The initial interface logic for the optocouplers is referenced to 28V. If multiple channels are active and large wattages are dissipated additional cooling will be required. Cooling can be though the chassis or direct air.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

https://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite B&C
Santa Cruz, CA 95060
831-457-8891
support@dyneng.com

Specifications

Host Interface:	[PC/104p] Mezzanine Card - 32 bit
Interface:	2 half duplex UARTs, 2 RX, 2 TX ARINC 429, 4-16 bit DAC, 4–16 bit ADC, 35 OptoCoupled inputs, 37 OptoCoupled outputs. Mixed High side and Low Side switches. Inputs have programmable COS detector circuits
Rates generated:	PCI clock plus 18.432 MHz oscillator, programmable 18 bit divider for programmable frequencies. Custom oscillators can be installed for alternate frequencies.
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses
Interrupt:	COS interrupt for Rising and/or Falling conditions UART interrupts for TX and RX 429 interrupts for TX and RX Software interrupt
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Connector	Multiple WDM Micro D connectors
Dimensions:	custom. Slightly larger than double PC/104 card. Approx. 6” x 9”
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.
Power:	Max. **TBD** mA @ 5V

Order Information

BaseBoard	6” x 9” double PC/104 with power conditioning, 35 OptoIsolated inputs, 37 Optocoupled outputs, 4 DAC, 4 ADC, 2 UART and 2 ARINC 429 channels implemented. PC104p-BaseBoard is configured as slot 0 in the PC/104p stack.