USER'S GUIDE

PCIeBPMCX1 - 4 PCIe Lane
PCIeBPMC – 1 PCIe Lane

PCIe and PMC Compatible Carrier

Document Revision 07p4
Corresponding Hardware: Revision 01- 15
Fab number:10-2007-07(1-15) for PCIeBPMCX1
Fab number:10-2008-070 (1-7) for PCIeBPMC

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Est. 1988

Design Revision History

Revision	Date	Description
Version 01	12/20/2007	New design
02	5/29/2008	Added EPAD voltage test points. Updated PCI_SEL_100 Default to 'No Delay' on Power Supplies.
03	3/9/2010	Updated power to use PowerPak FET's and increase current.
04	4/26/2010	Added input side capacitance to compensate for cable'd 12V input power at high loads.
05	10/15/2010	Fab level only for FAN cutout update
06	10/15/2010	Added DIODE at 1744 ckt per Maxim. Added voltage monitor ckt.
07	03/19/2012	Minor package changes. Adjust rail break-offs.
08	09/13/2012	Switch to 0402s
09	10/31/2013	Maintenance revision - no schematic changes - footprints in layout
10	5/15/2015	Added headers for power supply start-up control.
11	3/22/2017	Removed blocking caps from REFCLK. Change values to .22 on rest.
12	3/25/2019	Update -12V supply. Switch Bridge due to EOL TSI device
13	1/24/2024	Minor update to Fan footprint
14	8/22/24	Minor clean-up and manufacturing updates
15	6/24/25	Update for revision 15 PCIeBPMCX1

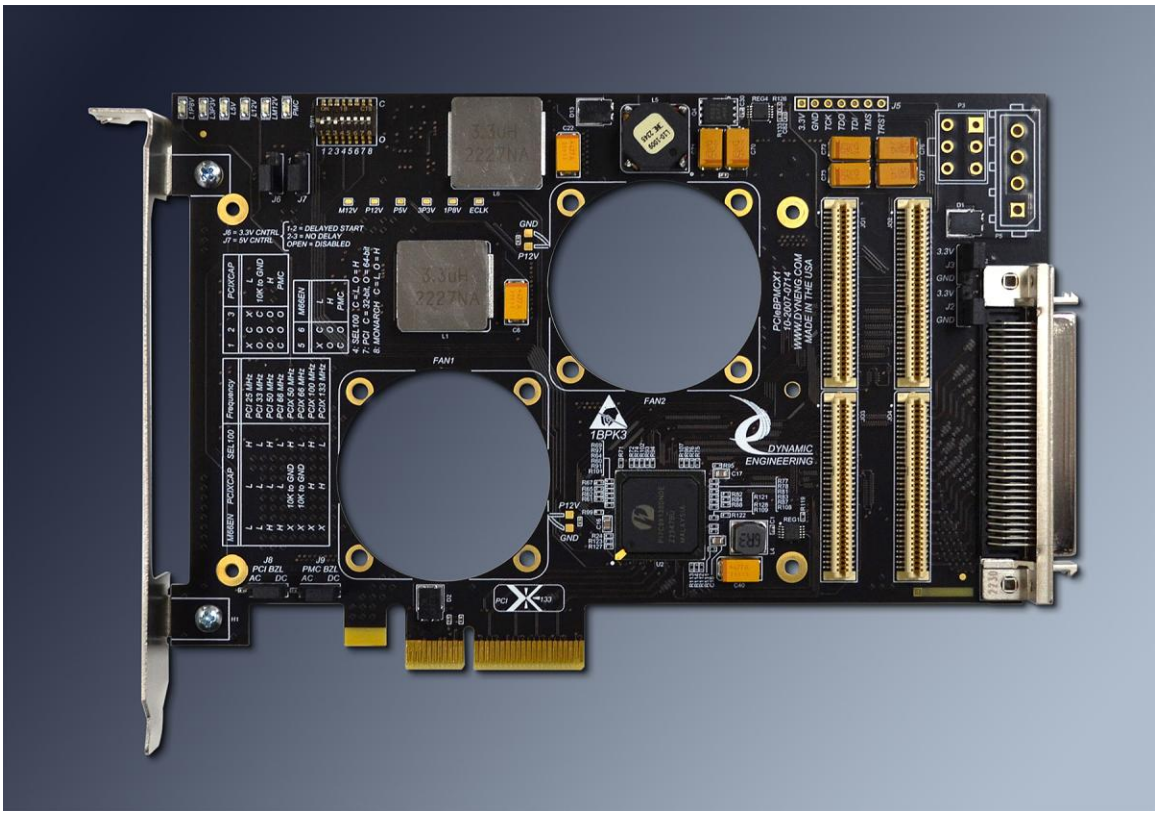
Document Updates

- Revised format and organization.

Note: Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The revisions shown are for the X1 models. The single lane version is updated from the four-lane version. Revision 7 is equivalent to Revision 15[X1].

PCIe, PCI and PMC Compatible Carrier



Rev 14 PCIeBPMCX1 shown.

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Cautions and Warnings

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user at their own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

Product Description

PCIeBPMCX1 and PCIeBPMC are part of the Dynamic Engineering PCI Express and PMC Compatible family of modular I/O components. PCIeBPMCX1 and PCIeBPMC adapt a PMC to PCIe. The X1 was launched in 2007 and the single-lane version in 2008, with thousands delivered.

The PMC, when mounted to PCIeBPMCX1, creates a stacked assembly that is PCIe-compliant in height with only one slot used. The Bezel IO on the PMC, if any, is available at the standard PC IO port, typically at the rear of the computer. User IO on connector Pn4 is available for internal routing, typically at the rear of the carrier card. A right-angle SCSI connector is standard. Vertical connectors can be installed.

PCIeBPMC utilizes one PCIe lane to operate with PCI(x)-25, 33, 50, 66 speeds. PCIeBPMCX1 uses up to four PCIe lanes to operate with PCI-25, 33, 50, 66, 100 or 133 speeds.

One-lane design can operate at any of the listed speeds. The one lane available may reduce the overall throughput depending on the application. Register accesses and other short-bursted activity may not be affected.

Four-lane design with longer DMA transfers at a high bandwidth is recommended.

Many PCs are supplied with more one-lane PCIe connectors than 4, 8 or 16 lane connectors. Many PMCs are 32/33 PCI implementations can use the single PCIe lane slot without any reduction in speed compared to using in a four PCIe lane position.

Both designs are the same, with the following differences:

- The number of lanes connected
- The mechanical size of the PCIe connector
- Tying the PRESENT signal to the 1 lane versus 4 lane

Table 1: PCIEBPMCX1 and PCIeBPMC Differences

	PCIe Connector size	PCIe Lane use	PCIe Lane connectors
PCIeBPMCX1	4 lane min. backplane connector size	up to 4 lanes used	=> 4, 8, 16 or 32 lane connectors can be used
PCIeBPMC	1 lane min backplane connector size	1 lane used	any lane count connector can be used

Unlike PCI, the PCIe specification provides for 12V power [only] to be used by the Express module. A minimal amount of 3.3V is available from the Express connector, but not enough to power typical PMC devices. Local power supplies operate from the +12V to create the rest of the PMC voltages [-12, 5V, 3.3V].

With revision 12 and later the 5V and 3.3V power supplies can source 15A each. Previous revisions support 9.5A. The -12V is designed for 4A, but effectively limited by the single pin assigned by the PMC specification. For higher current requirement modules, the **Zero Slot** FAN options are recommended.

With revision 15/7 the power to the bridge [3.3V] was removed from the gold fingers and added to the internal power supply. Since this power supply is now required for operation the selection for on/off & immediate/delayed was moved to the -12V supply. Some of the newer "server" designs have sequenced power supplies which can create an issue with the installed PMC for enumeration. Removing the 3.3V dependency cures this issue.

The transparent bridge does not require any software interaction. When hosted by the PCIeBPMC or PCIeBPMCX1, your PMC drivers will work without modification. If settings are adjusted, the bridge can provide higher bandwidth for DMA transfers. Contact Dynamic Engineering for information about modifications.

PCIeBPMCX1 was tested using PMC-BiSerial-VI-UART configured to perform internal loop-back transfers using DMA and Version 5.3.0 Linux Kernel. PMC-BiSerial-VI-UART has 8 ports each with separate transmit and receive DMA transfer engines. In addition, the design supports internal loop-back between the transmit and receive memory for each port.

The test ran continuously over a six-day period. The average transfer rate was 59.2mb/s (7.4mb/s per channel) with no errors. The total data transferred was approximately 30TB.

note: these tests were run on a previous revision carrier. When we have a chance to re-run the tests we will update this note for conditions and results.

For more information about PMC-BiSerial-VI-UART and other designs based on PMC-BiSerial-VI, refer to: www.dyneng.com/PMC-BiSerial-VI.html

Key Product Features

The table below lists the default and optional product feature:

Table 2: Product Features

Feature	Comments
PCIe Compliant 1 - 4 lane design based on highest performance bridge	
PCI, PCI-X compliant on secondary [PMC] bus	
LED on PMC Busmode "Present"	
LEDs on plus 12V, minus 12V, plus 5V, plus 3.3V plus bridge power.	Each is controlled by a voltage monitoring circuit. If illuminated the voltages are within tolerance.
Local power supplies for +5, 3.3 and M12	With revision 10 boards, the 5V and 3.3V supplies can be disabled, delayed, or instant on. With revision 12 the power supplies source up to 15A ea. With revision 15 the 3.3V is no longer selectable in favor of M12V.
VIO set to 3.3V	
32 or 64 bit operation	
133, 100, 66, 50, 33 or 25 MHz operation	Can be user-selected or automatic. I lane board limited to 33 MHz and below.
Front panel connector access through PCIe bracket	
User I/O [Pn4] available through SCSI II connector.	Routing done as matched length, differential pairs with 100 Ω differential impedance. Spare pins on SCSI connector can be shunt selected to power or ground.
Cooling cutouts for increased airflow to PMC	Options to install fans when required.
Optional Fan(s) for increased airflow, both positions have "zero slot" height feature	
Optional JTAG programming support	
Clearance for XMC connectors [rev 2 and later boards]	
User Selection for AC, DC and open for both PMC Bezel and PCIe Bezel	

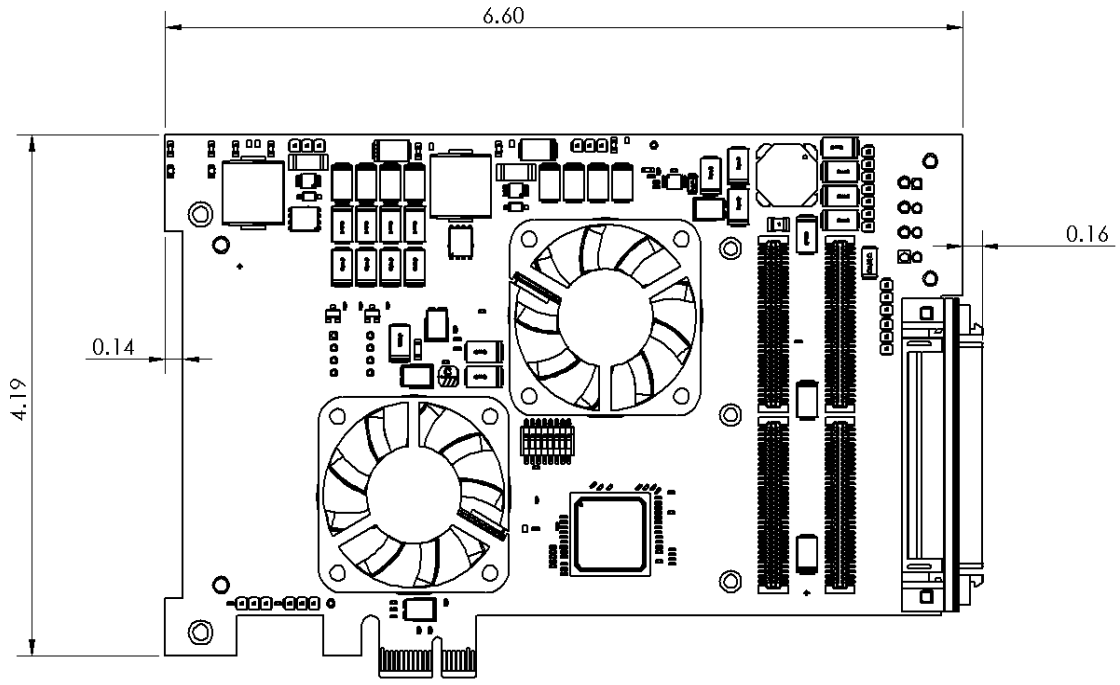
Product Specifications

Table 3: Product Specifications

Logic Interfaces	PMC: PCI, PCI-X Interface PCIe: 1-4 lanes
Access types	PCI bus accesses
CLK rates supported	133, 100, 66, 50, 33, 25 MHz PCI clock rates
Bus Size Supported	32- or 64-bit wide operation
Software Interface	Transparent Bridge. PI7C9X130DNDE registers in configuration space. Access to registers is usually not required.
Initialization	Dipswitch settings for optimized performance. Factory defaults usually best choice. No software required to operate transparent bridge.
Interface	PMC front bezel via PCI bracket and User I/O connector via SCSI II connector.
Dimensions	1/2 length PCIe board. Single PCIe slot width with PMC installed.

PCIeBPMC Outline Drawing

Figure 1: Revision 05 Single-lane Version, Top View Dimensions



PCIeBPMC Top View Dimensions

For current models please contact Dynamic Engineering. Step files are available.

Installation and Interfacing Guidelines

Some general interfacing guidelines are presented below. If you need more assistance, contact Dynamic Engineering.

Installation

Warning: Connection of incompatible hardware is likely to cause serious damage.

PCIeBPMCX1 is ready to use with the default settings. Just install the PMC onto the PCIeBPMCX1 and then into the system. To change the default settings, refer to the sections on DipSwitch settings and Pin assignments.

The PMC is mounted to the PCIeBPMCX1 prior to installation within the chassis. For best results, with the PCIe bracket installed, install the PMC at an angle so that the PMC front panel bezel penetrates the PCIe bracket. Then rotate down to mate with the PMC [PnX] connectors.

There are four mounting locations per PMC. Two into the PMC mounting bezel and two for the standoffs near the PMC bus connectors.

Start-up

Make sure that the system is visible to your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the *VendorID* and *CardId* for the PMC installed and an interrupt level. If the information is not available from the OS, then a third-party PCI device cataloging tool will be helpful. The device manager can be used for Microsoft Windows OS installations. lspci command can be used in Linux systems.

Guidelines

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCIeBPMCX1 when it is not powered can damage it and the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the PMCs installed onto the PCIeBPMCX1 than the PCIEBPMCX1 itself and it is good system design when it can be achieved.

Thermal Considerations

If the PMC installed has large heat dissipation, forced air cooling is recommended. A fan option is available for high thermal load PMCs or for a chassis with a lack of air circulation. The fan option is required for PMCs using 5A or more on either or both of the 5V or 3.3V rails.

DipSwitch Settings

The dipswitch is numbered SW1 and is located near the center of the board. SW1 controls the Bridge operation.

UP = Closed
DOWN = Open.

Note: Switch numbering and 'C' and 'O' definitions are per the silk screen.

Forced Operation Settings

Note: The PMC must be capable of operating at the selected frequency. To force frequency selection independent of the PMC, open switch 1 and 5. *Opening these switches* separates frequency selection from the installed PMC. Opening the switches and using the table settings forces the frequency. Closing 1 and 5 and opening the other switches places the PMC in charge.

Table 4: Forced Operation Settings

Mode and Bus Rate	PCI_PCIXCAP	PCI_SEL100	PCI_M66EN
	Switches		
	1,2,3	4	5,6
PCI 25 MHz	O,C,C	O	O,C
PCI 33 MHz	O,C,C	C	O,C
PCI 50 MHz	O,C,C	O	O,O
PCI 66 MHz	O,C,C	C	O,O
PCI-X 50 MHz	O,O,C	O	O,O
PCI-X 66 MHz	O,O,C	C	O,O
PCI-X 100 MHz	O,O,O	O	O,O
PCI-X 133 MHz	O,O,O	C	O,O

Automatic Operation Settings

Table 5: Automatic Frequency Selection

Mode and Bus Rate	PCI_PCIXCAP	PCI_SEL100	PCI_M66EN
	Switches		
	1,2,3	4*	5,6
Automatic selection	C,O,O	C/O	C,O

***Note:** Switch 4 is used to select between the upper and lower frequency at each frequency level (25/33, 50/66, 100/133).

Bridge Special Selections

The DIPSWITCH has 8 switches. Normal IC pin numbering is used. 1-16 comprise switch 1, 2-15 => switch 2 and so on.

Factory default is "C O O O C O C C"
C= closed [on], O = Open [not on]. 1-8

For more information, refer to the Pericom documentation for the bridge.

ON is marked on the switch near pin 16.

Position 1 corresponds to S_PCIXCAP and P_PCIXCAP. When closed, the signals are tied together. When open, the signals are isolated. The S_PCIXCAP is tied to the PMC position PCIXCAP signal. P_PCIXCAP is tied to the Bridge. When connected together automatic operation is enabled. The PMC and Bridge negotiate for the frequency automatically. Setting to open isolates the two devices and allows the user to override the PMC set-up.

DIPSWITCH pins 16, 15, and 14 are tied together to allow the user to control the bridge side of PCIXCAP with options on switches 1, 2, 3. Connecting the signals through on **switch 1** and leaving switches 2, 3 open is the default setting for standard operation.

Closing **switch 2** can be used to ground the Bridge side PCIXCAP signal and selectively ground the PMC version of the signal if position 1 is also closed. This has the effect of forcing the speed range to be 25-66 MHz.

Closing **switch 3** can be used to create an intermediate voltage on the PCIXCAP signal on the Bridge and optionally on the PMC side. There is a 56KΩ pull-up to 3.3 on the secondary side of the switch. Closing switch 3 adds the pull-down resistor – 10KΩ to ground. PMCs with PCI-X 66 capability should have the 10 KΩ pull-down on the PMC making the intermediate voltage selection automatic.

PMC cards operating at PCI 66 MHz [not PCI-X] will ground the PCIXCAP signal and leave M66EN high. The ground from the PMC will override the switch 3 setting unless switch 1 is open.

Switch 4 when open leaves PCI Select 100 pulled up to 3.3 though an 8.2KΩ resistor. If the switch is closed the signal is tied to ground.

Note This feature was added for revision 2 and later boards.

PCI Select 100 is used to toggle between 100 and 133 or 50 and 66 or 25 and 33. The default selection is closed to allow the PMC to select 33, 66, or 133 MHz.

Switch 5 and **Switch 6** correspond to S_M66EN [PMC] and P_M66EN [bridge] respectively.

In the default setting, Switch 5 is closed and Switch 6 is open. The signals are connected together with a light pull-up on each side. When Switch 6 is closed, the Bridge side is forced to ground – low speed operation.

When switches are open, the signal is 1, assuming that the PMC does not pull the signal down. S_M66EN/P_M66EN acts as an open drain signal with any of the nodes capable of reducing the clock rate and all nodes required to operate at the higher rate.

Select the secondary side [PMC] PCI bus frequency. With the PCIe to PCI bridge, the PCI clock is not related to the PCIe rate. The switches and card pin strapping control the frequency. Tying the M66EN between the bridge and PMC plus doing the same for the PCIXCAP signal will allow for automatic clock selection based on the PCI/PCI-X specifications.

Position 7 corresponds to Device 64. When closed, the PCI bus operation is set to 32 bit. When open the PCI bus is set to 64 bit. Most PMC boards are 32 bit. The default is closed. Note: this signal was PLL Enable on revision 1-11 PCIeBPMCX1 and Rev 1-6 of PCIeBPMC.

Position 8 is used to ground the Monarch pin J2-64. A pull-up holds the signal high, when the switch is not closed. Closing the switch grounds the signal. Refer to the installed PMC vendor documentation for details relating to this signal.

Interrupts

Interrupts from the PMC are connected from the PMC to the primary PCIe bus. INTA through INTD are connected to the bridge, where the interrupt requests are mapped into PCIe control words and sent to the host computer. The host will respond over PCIe as programmed by the user software to process the interrupt.

IDSEL Setting

IDSEL is set to AD20 for the PMC slot [secondary PCI].

PMC Interface, Jn2 pins

Jn2 pins 58 and 64 are pulled up to VCC_IO with 4.7KΩ. Pin 60 is open. This configuration works with most Monarch-capable PMCs. Please contact Dynamic Engineering if you need alternate settings. The monarch pin is also tied to the DIPSWITCH for user selection.

Fan Options

PCIeBPMCX1 features cooling cutouts designed to support the addition of a fan in one and/or two positions for the PMC. On PrPMCs, and other PMCs, with high thermal loads, the fan option is recommended. On cards with a lower thermal profile, the fan(s) are unnecessary.

The fan produces ~5 CFM in a small area to create a high LFM rating suitable for most cooling requirements. The fan used has a relatively low noise rating for quiet operation. Position 1 is closest to the PCIe bezel and position 2 is closer to the PMC connectors.

The fan positions are designed to enable the fan to be mounted through the PCB. The thickness of the PCB is used to reduce the overall thickness of the fan. By doing so, fans can be used and be permitted for a height [less than .105”] on the rear of the card. Both fan positions are located outside of the connector area. With fans installed, the full free space height of 4.7mm is permitted.

Note: the full 10mm is available within the entire connector area, with or without fans.

For a complete list of fan options, refer to *Ordering Information* at the end of this document or online at:

4-PCIe lane connector: www.dyneng.com/pciebpmcx1.html

1 PCIe lane connector: www.dyneng.com/pciebpmc.html

Construction and Reliability

PCIeBPMCX1 is constructed out of 0.062-inch-thick High Temp FR4 ROHS compliant material. Cooling cutouts have been designed into the product for improved airflow to the PMC sites. The components on the PCIeBPMCX1 are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in the situation when a large portion of the board has little or no power dissipation.

Surface mounted components are used. The connectors are SMT for the PMC bus and through hole for the IO.

The PMC Module connectors are keyed and shrouded with gold-plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent and correct insertion easy and reliable.

The PMC Module is secured against the carrier with the PMC connectors. For enhanced security against vibration, it is recommended that the PMC mounting screws are installed.

Note: Screws are supplied with the PMC from the OEM. if your PMC is missing some of the required attachment hardware, Dynamic Engineering has screws, standoffs, blank bezels and other PMC hardware available at a reasonable cost.

Power Supplies

In many PCIe implementations, smaller lane count boards do not provide enough power to the main PCIe connector.

12V, 3.3V, and 3.3V AUX are available on the backplane connector.

PCIeBPMCX1 uses the 12V and 3.3V for internal functions. For revisions below 15 The 3.3V rail is used for the bridge and not connected to the PMC. The PCIe 12V is also used to generate the 1.8V for the Bridge. With Revision 15, the bridge 3.3V also comes from the 12V input.

12V is Diode coupled to a second optional power connector located at the rear of the card. For applications requiring more than ~60W total power consumption, the rear connector should be added.

The 12V rail is tied to PMC 12V and to the power supplies that generate the M12, 5V, 3.3V.

The 12V input rail at the gold finger connector is limited to about 5.5A max. 66W is the maximum input power. The power supplies have been measured to be about 90% efficient, leaving 59.4W for internal use. The bridge can use up to 2W, leaving a minimum of 57.4W for the PMC.

The 5V and 3.3V supplies can generate 15A each, exceeding the capacity of the 12V input rail. Due to pin limitations on the PMC connector. minus 12 has excess capacity and will likely be limited to 1A. +12V also shares this situation.

For designs using less than 5A on the 5V and 3.3V rails and operating in a “lab” environment, no additional cooling is required. With loads approaching 5A and/or operating at higher temperatures, or for bards with hot spots, forced air cooling is required.

The zero slot fans provide enough air flow to extend the operational limit of the supplies. The full 15A may require additional airflow to the rear of the card depending on the operational temperature etc.

Note: For revision 3 and later boards, the FETs were changed to a different package. The Drain is tied to a pad on the bottom of the part, allowing direct thermal contact. The improved package reduces the thermal resistance sufficiently to move the max no air flow current rating. In addition, the inductor and FET have improved characteristics, allowing for a max of 15A.

3.3 AUX is directly routed to the PMC on the 3.3V AUX pin.

Power Supply Configuration

Many implementations will stay within the 57.4W limitation. For those designs requiring extra power, there are two basic options to select from:

- The “AP” connector to mate with 6 pin PC power supply wiring harness connector
- The ‘DDV” to mate with the traditional Disk Drive 4 position PC power supply wiring harness

Three connector options are available for revision 2 boards and later:

Option 1: –DDV for a “Disk Drive” style vertical connector that will mate with the standard 4 pin HDD cable. Each pin can handle 5A. There is 1, 12V pin on this style connector, allowing an additional 60W to be input to the board. This connector supplied for legacy ordering.

Option 2: The –AP version mates with the 6 pin standard PC power cable. 3 12V pins and 3 grounds in this configuration. 13A per pin rating. This connector will provide maximum additional power.

Option 3: With revision 10 [X1] and 5[1 lane] two additional 3-pin headers are added to the design. **J6** controls the 3.3V supply and **J7** controls the 5V supply. With no shunt installed, the power supplies are disabled. If your PMC does not use the 3.3V or 5V power, it is recommended to remove the corresponding shunt.

Note: Since the power is out of tolerance in this configuration, the corresponding LED will go dark.

When 1-2 are connected, the power supply is enabled with a delayed start-up. When 2-3 are connected, the power supply is enabled without a delay.

The headers are labeled in the silk-screen. If you need a second indicator, the square pad is pin 1.

The delay waits for the +12 to reach approximately 5V before starting a supervisor circuit timer. The circuit adds an additional delay before enabling the power supply. The delay can reduce the system in-rush requirement.

Note: In some systems the enumeration happens early and the installed PMC may need the instant on setting to be configured in time to be enumerated correctly.

You can see the affect by delaying one supply and not the other, powering on and looking at the monitor LEDs.

Pinout Options

P3, P5 Power Pinout

Table 6: Secondary Power Connections

NAME	P3	P5
GND	4,5,6	2,3
+12	1,2,3	1
+5	NA	4

Note: The 5V power on P5 is not used by PCIeBPMCX1.

P5 = -DDV option vertical mount Disk Drive style connector to mate with standard PC HDD power cable

P3 = -AP option 6 position power style connector to mate with standard PC power supply cable.

J8, J9 Bezel Reference Pinout

Located low on the card near PCIe bezel.

J8 and J9 are used to select the grounding option for the PCIe and PMC Bezels respectively. The silk-screen shows AC and DC positions for a shunt to select:

AC = .1 uF cap to ground

DC = direct connection to ground

No shunt = open connection to ground

Note: Frequently, it is best to DC couple on one side and AC on the other side of a common cable to provide a reference for the cable shield and prevent ground loops.

J2, J3 SCSI Power Pinout

Located at the rear of the card next to the SCSI connector.

J2 and J3 are three pin headers used to select the definition of pins 33,67(J2) and 34,68(J3) on the SCSI connector. The headers are installed if the –SCSI option is selected when ordering. Shunting pins 1-2 applies 3.3V, 2-3 applies ground. The silk-screen shows 3.3 and GND positions for a shunt to select No shunt = open connection. The pins and shunts can handle slightly under 1A per header. Not fuse protected.

PMC Module I/O Interface

The table below provides the pin assignments for the PMC Module I/O Interface pin assignment – from Pn4 to the PCIeBPMCX1 connectors.

Table 7: PCIEBPMCX1 PN4 Interface Standard

SCSI II [P2]		Pn4	
35	36	1	2
1	2	3	4
37	38	5	6
3	4	7	8
39	40	9	10
5	6	11	12
41	42	13	14
7	8	15	16
43	44	17	18
9	10	19	20
45	46	21	22
11	12	23	24
47	48	25	26
13	14	27	28
49	50	29	30
15	16	31	32
51	52	33	34
17	18	35	36

Continued			
SCSI II [P2]		Pn4	
53	54	37	38
19	20	39	40
55	56	41	42
21	22	43	44
57	58	45	46
23	24	47	48
59	60	49	50
25	26	51	52
61	62	53	54
27	28	55	56
63	64	57	58
29	30	59	60
65	66	61	62
31	32	63	64
33	67 Open, +3.3 or GND via J2 silk screen defined		
34	68 Open, +3.3 or GND via J3		

Figure 1: PCIEBPMCX1 PN4 Interface STANDARD

Read table:
P2-1 = Pn4-3
P2-35 = Pn4-1
etc.

Signals are matched length and differentially routed with 100 ohm impendance.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

Contact

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Order Information

Standard temperature range **–40 - 85ºC** rated components

PCIeBPMCX1	4 PCIe lane connector. 1-4 lane operation. Compatible with 4 or more lane backplane connectors. www.dyneng.com/pciebpmcx1.html
PCIeBPMC	1 PCIe lane connector, 1 lane operation. Compatible with 1 or more lane backplane connectors www.dyneng.com/pciebpmc.html **Common Features** 1/2 length PCIe adapter with PMC positions **Options:** –FAN1, -FAN2, -FAN12, -FAN1R, -FAN1R2 **1** or **1RZ** fan position 1 for low profile or rear mount only **2** or **2RZ** fan position 2 for low profile or rear mount only **1R** 8CFM fan position 1 for R mount only **2R** 8CFM fan position 2 for R mount only **-NC** no SCSI connector installed **-ROHS** for ROHS compliant processing **-CC** add Conformal Coating **-5VXXX** 5V supply forced to (replace XXX) [ND], [DEL], [OFF] **-DDV** add vertical disk drive power connector **-AP** add high power connector – 6 position PC power cable
HDEterm68	68 pin SCSI II to 68 screw terminal converter www.dyneng.com/HDEterm68.html
HDEcabl68	68 pin SCSI cable available in several lengths www.dyneng.com/HDEcabl68.html