User Manual

PIM-Parallel-IO

PMC I/O Module for PMC-Parallel-TTL & PMC-Parallel-IO

PIM with SCSI Bezel Connector

Manual Revision	**02p1**
Revision Date	**8/26/2020**
Corresponding Hardware	**10-2001-05(01-02)**
Current Fab Number	**10-2001-0502**

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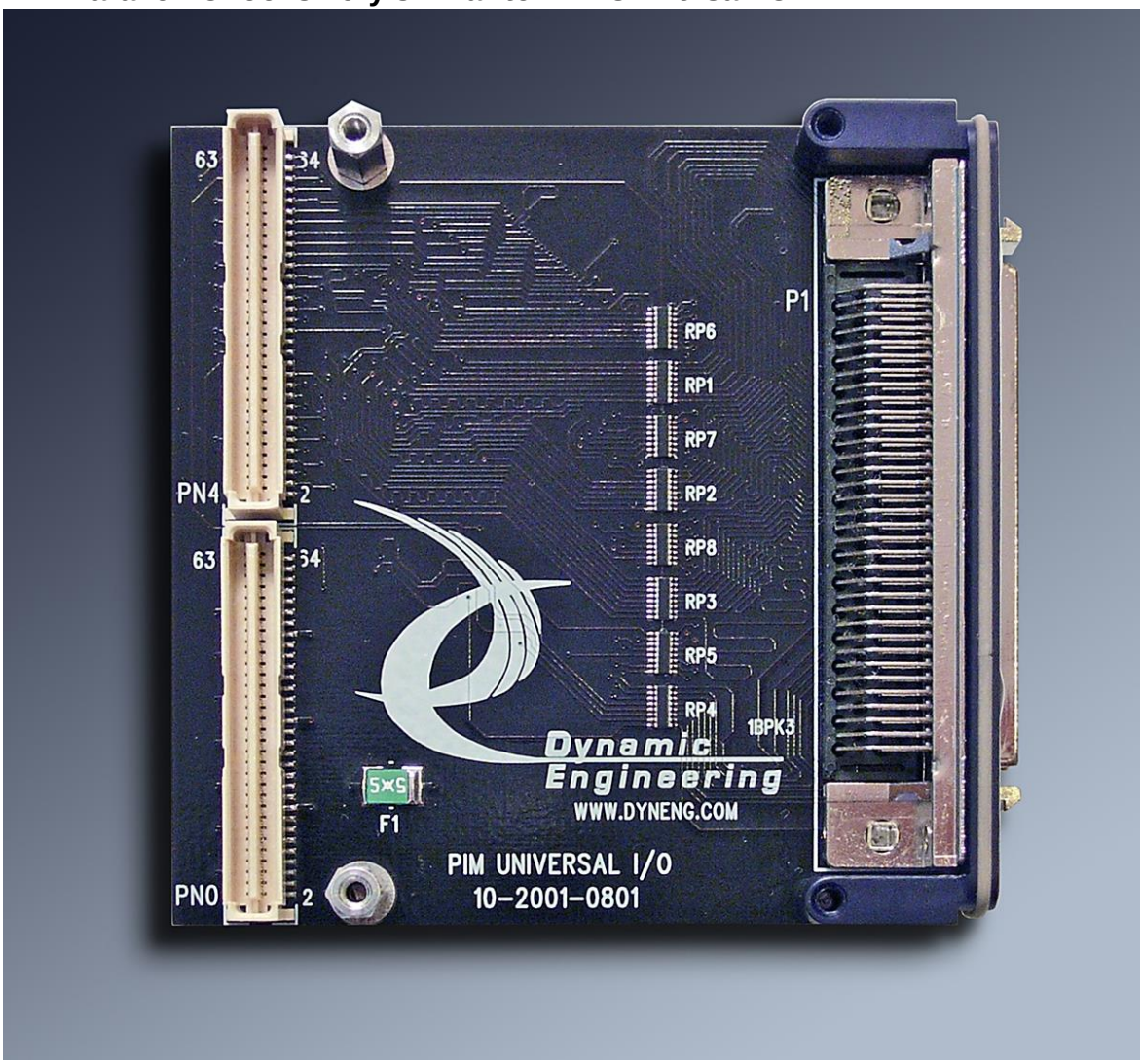
Est. 1988

PIM-Parallel-IO looks very similar to PIM-Universal-IO



Cautions and Warnings

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at their own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without express written approval from the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

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Design Revision History

Table 1: Design Revision History

Revision	Date	Description
A	2/26/2001	Initial release of design
B	3/30/2001	Added fused power to unused pins on P1

Manual Revision History

Table 2: Manual Revision History

Revision	Date	Description
NOTE: Revisions released prior to August 2020 may have incomplete data		
A	9/5/2001	Initial Manal Release
02p1	8/24/2020	Updated formatting to improve usability

NOTE: Dynamic Engineering has made every effort to ensure that this manual is accurate and complete; that being said, the company reserves the right to make improvements or changes to the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

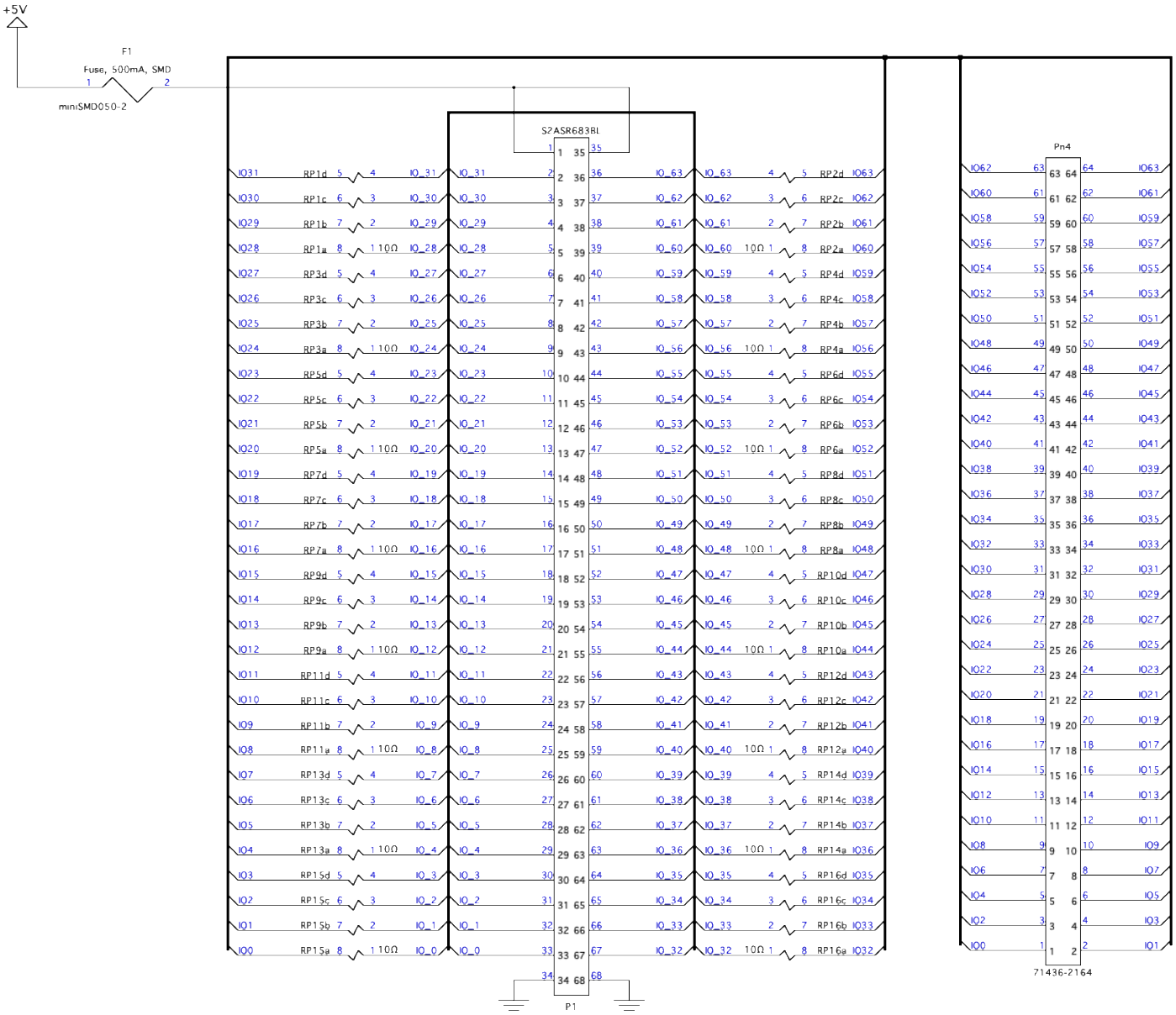
Product Description

PIM-Parallel-IO is part of the PMC Module family of modular I/O components. The purpose of the PIM-Parallel-IO is to facilitate rear panel I/O. The Pn4 user I/O on the PMC is routed through the host carrier board to the backplane. A PIM Carrier is mounted to the underside of the backplane. The Pn4 I/O is passed through the backplane connectors to the PIM carrier and to the installed PIM devices. When installed, PIM-Parallel-IO will recreate the PMC-Parallel-IO and the PMC-Parallel-TTL front bezel I/O in the rear compartment of the chassis (under the backplane). All of the 64 I/O connections are routed to the 68-pin SCSI II connector. The signals are routed through 0 Ohm resistors. Alternate values can be implemented if desired.

The PIM specification provides for power and ground references. The ground reference is used to tie into internal planes used as references for the signals routed across the PIM.

The bezel, connector, and connections are the same as the PMC-Parallel-IO and PMC-Parallel-TTL to allow the same cables to be used on the front panel bezel or the PIM bezel. The only exception being the signals on pins 1,35 of the SCSI connector, which are not available on the Pn4 connector. Pins 1 and 35 are connected to 5V via a resettable fuse. All 64 I/O are available. Two signal grounds are provided. Please refer to the PIN assignment tables for connector definitions.

Figure 1: PIM-Parallel-IO Schematic



Key Product Features

Table 3: Key Product Features

Feature	Description
Signal Routing	Use PIM to route PMC/XMC signals for rear panel applications
Controlled I/O	Matched-length, impedance-controlled I/O
Optimized	Optimized for PMC-Parallel-IO and PMC-Parallel-TTL
SCSI	SCSI connector at rear bezel (SCSI cables and DIN Rail breakouts available)

Product Specifications

Table 4: Product Specifications

Specification	Description
Carrier Connector	PMC Pn4 Connector
Bezel Connector	SCSI II connector with latch-blocks
I/O	64 I/O routed plus two additional ground and two additional 5V connections 0, 10, 22, 33 Ohm series resistors in signal path between Pn4 and P1

Construction and Reliability

PIMs are conceived and engineered for rugged industrial environments. The PIM-Universal-IO is constructed out of 0.062-inch thick, high-temp FR4 material.

Through-hole and surface mounting of components are used. High insertion and removal forces are required, which assists in the retention of components. The stand-offs should be used to mount the PIM to the PIM carrier to provide added protection against vibration induced intermittent connections.

The PMC Module connectors are keyed and shrouded with Gold-Plated pins on both plugs and receptacles. They are rated at 0.5 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PIM-Parallel-IO is entirely passive.

Installation and Interfacing Guidelines

Some general interfacing guidelines are presented below. If you need more assistance, contact Dynamic Engineering.

Installation

Warning: Connection of incompatible hardware is likely to cause serious damage.

ESD

Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within 0.7 volts of ground potential.

Guidelines

Grounds - Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should have all their own ground wires back to a common point.

Pin Assignments

PIM Module Front Panel I/O Interface Pin Assignment

The table below gives the pin assignments for the PIM Module I/O interface on the PIM-Parallel-IO.

Table 5: PIM-Parallel-IO Bezel

Signal Names		P1 SCSI	
Fused 5V	Fused 5V	1	35
IO_31	IO_63	2	36
IO_30	IO_32	3	37
IO_29	IO_31	4	38
IO_28	IO_60	5	39
IO_27	IO_59	6	40
IO_26	IO_58	7	41
IO_25	IO_57	8	42
IO_24	IO_56	9	43
IO_23	IO_55	10	44
IO_22	IO_54	11	45
IO_21	IO_53	12	46
IO_20	IO_52	13	47
IO_19	IO_51	14	48
IO_18	IO_50	15	49
IO_17	IO_49	16	50
IO_16	IO_48	17	51
IO_15	IO_47	18	52
IO_14	IO_46	19	53
IO_13	IO_45	20	54
IO_12	IO_44	21	55
IO_11	IO_43	22	56
IO_10	IO_42	23	57
IO_9	IO_41	24	58
IO_8	IO_40	25	59
IO_7	IO_39	26	60
IO_6	IO_38	27	61
IO_5	IO_37	28	62
IO_4	IO_36	29	63
IO_3	IO_35	30	64
IO_2	IO_34	31	65
IO_1	IO_33	32	66
IO_0	IO_32	33	67
GND	GND	34	68

PIM Module Pn4 I/O Interface Pin Assignment

The table below gives the pin assignments for the PIM Module I/O interface on the PIM-Parallel-IO and routed from Pn4. Also see the user manual for your carrier board for more information.

Table 6: PIM-Parallel-IO Pn4 Interface

Signal Names		Pn4	
IO_0	IO_1	1	2
IO_2	IO_3	3	4
IO_4	IO_5	5	6
IO_6	IO_7	7	8
IO_8	IO_9	9	10
IO_10	IO_11	11	12
IO_12	IO_13	13	14
IO_14	IO_15	15	16
IO_16	IO_17	17	18
IO_18	IO_19	19	20
IO_20	IO_21	21	22
IO_22	IO_23	23	24
IO_24	IO_25	25	26
IO_26	IO_27	27	28
IO_28	IO_29	29	30
IO_30	IO_31	31	32
IO_32	IO_33	33	34
IO_34	IO_35	35	36
IO_36	IO_37	37	38
IO_38	IO_39	39	40
IO_40	IO_41	41	42
IO_42	IO_43	43	44
IO_44	IO_45	45	46
IO_46	IO_47	47	48
IO_48	IO_49	49	50
IO_50	IO_51	51	52
IO_52	IO_53	53	54
IO_54	IO_55	55	56
IO_56	IO_57	57	58
IO_58	IO_59	59	60
IO_60	IO_61	61	62
IO_62	IO_63	63	64

PIM Module Pn4 to Bezel Interconnect

The table below provides a reference for the signal routing from Pn4 to the bezel on the PIM-Parallel-IO card. When the PIM is used with PMCs other than the PMC-Parallel-IO, the table can help to create a transition table for the I/O.

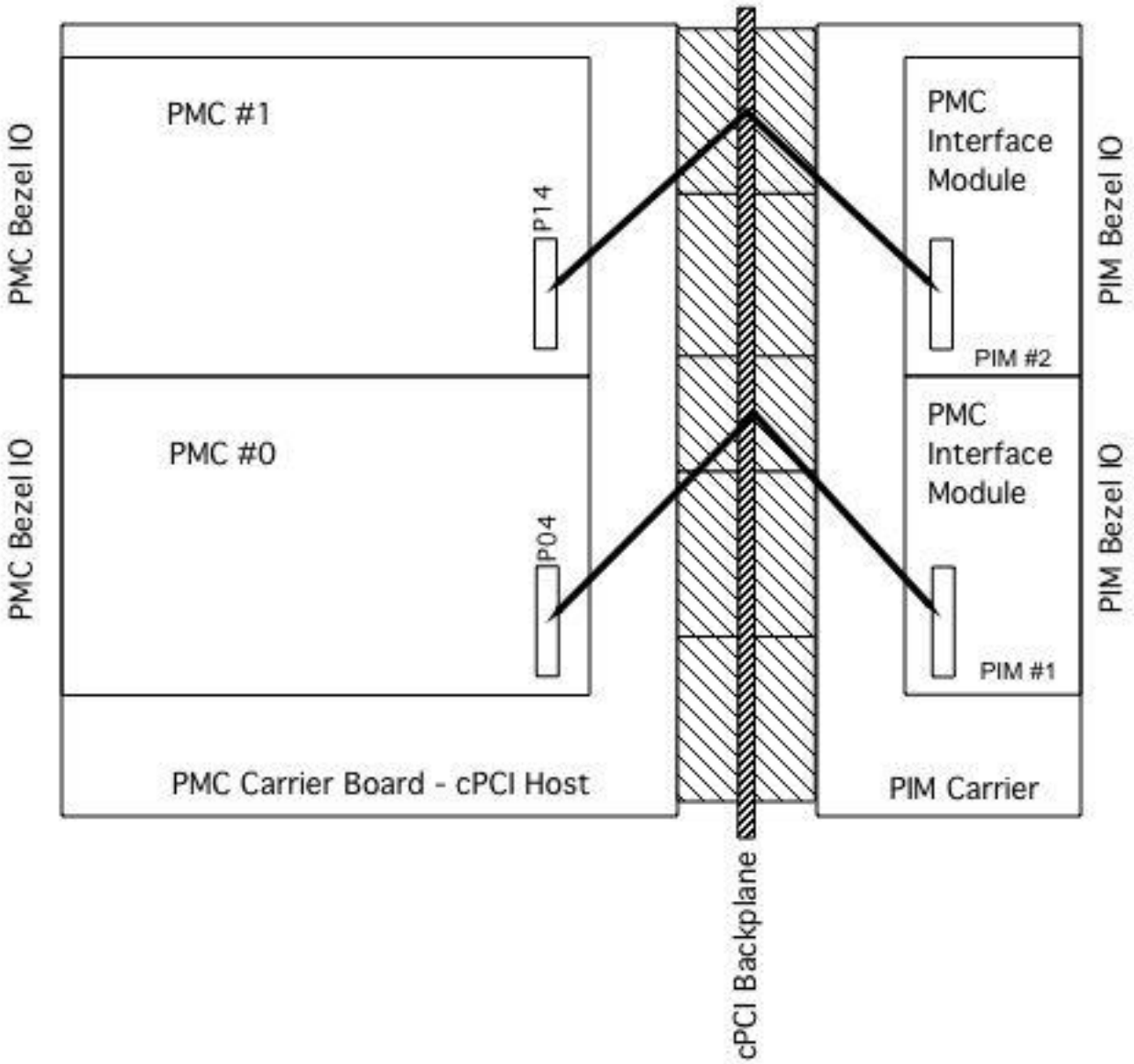
Table 7: PIM-Parallel-IO Interconnect Table

SCSI Connector P1			Pn4	
33	32		1	2
31	30		3	4
29	28		5	6
27	26		7	8
25	24		9	10
23	22		11	12
21	20		13	14
19	18		15	16
17	16		17	18
15	14		19	20
13	12		21	22
11	10		23	24
9	8		25	26
7	6		27	28
5	4		29	30
3	2		31	32
67	66		33	34
65	64		35	36
63	62		37	38
61	60		39	40
59	58		41	42
57	56		43	44
55	54		45	46
53	52		47	48
51	50		49	50
49	48		51	52
47	46		53	54
45	44		55	56
43	42		57	58
41	40		59	60
39	38		61	62
37	36		63	64
1	35	Fused 5V		
34	68	GND		

System Diagram

The figure below shows the relative connections of the PIM installed into the PIM carrier. The carrier attached to the rear of the backplane and the host to the front of the backplane. The PMC is attached to the host. The Pn4 I/O is routed from the PMC to the PIM to provide the PIM Bezel I/O. With the PMC and PIM-Universal-IO combination, the Pn4 I/O is the same for the 64 I/O signals on the two connectors. If the PIM-Parallel-IO is used with another PMC, the routing tables will need to be consulted to see what the pin definitions are for the PIM Bezel I/O.

Figure 2: PIM-Parallel-IO System Diagram



Warranty and Repair

Please refer to the warranty page on our website for the warranty and options that are currently offered.

www.dyneng.com/warranty

Service Policy

Before returning a product for repair, verify to the best of your ability, that the suspected unit is as fault. Then call the Dynamic Engineering Customer Service Department for a Return Material Authorization (RMA) number. Carefully package the product, in the original packaging if possible, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by anyone other than the original customer will be treated as out-of-warranty.

Out-of-Warranty Repairs

Out-of-warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the list price for one of that kind of unit. Return transportation and insurance will be billed as part of the repair in addition to the minimum RMA charge.

Contact:

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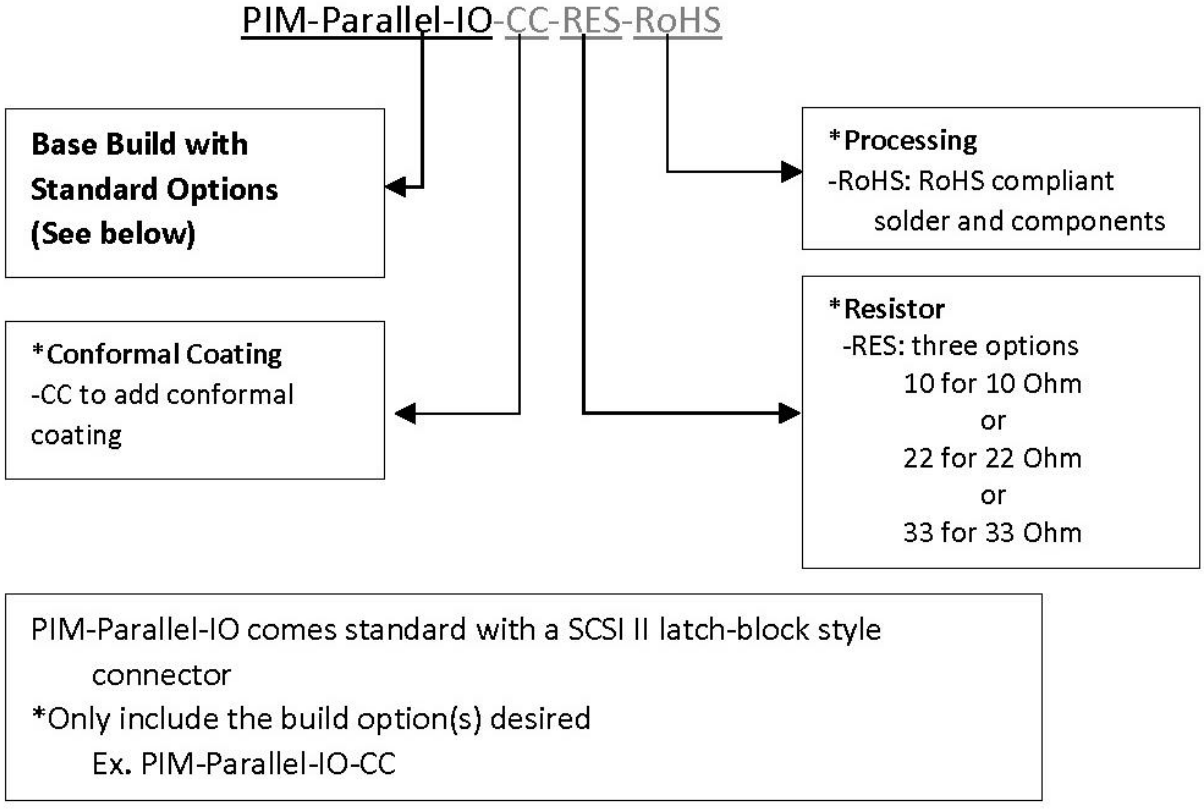
Ordering Information

Standard Temperature Range-Rated Components: -40 - 85°C

Table 8: Ordering Information

Product	Description	
PIM-Parallel-IO	PIM with SCSI II latch-block style connector.	
PIM-Parallel-IO	**Options:**	
	-RES	Three alternate series resistor value options available by special request 10 Ohm, 22 Ohm, or 33 Ohms
	-RoHS	Use RoHS processing. Standard processing is “leaded.”
	-CC	Option to add conformal coating
SCSI Cable: HDEcabl68	HDEcabl68 provides a SCSI compliant cable with either latch block or screw terminal retention. www.dyneng.com/HDEcabl68	
HDEterm68	SCSI II cable interface to 68-screw terminals. Comes with DIN rail mounting capability www.dyneng.com/HDEterm68	

Figure 3: Ordering Options PIM-Parallel-IO



Dynamic Engineering PIM-Parallel-IO Ordering Options Revision 01, August 26, 2020

Glossary

Baud	Used as the bit period when talking about UARTs; Not strictly correct, but is the common usage when talking about UARTs.
CardID	Unique number assigned to a design to distinguish between all designs of a particular vendor
CFM	Cubic feet per minute
FIFO	First In First Out memory
Flash	Non-volatile memory used on Dynamic Engineering boards to store FPGA configurations or BIOS
JTAG	Joint Test Action Group – a standard used to control serial data transfer for test and programming operations.
LFM	Linear feet per minute
LVDS	Low Voltage Differential Signaling
MUX	Multiplexor – multiple signals multiplexed to one with a selection mechanism to control which path is active.
Packed	When UART characters are always sent/received in groups of four, allowing full use of host bus/FIFO bandwidth.
Packet	Group of characters transferred. When the characteristics of the group of characters is known, the data can be stored in packets and transferred as such; the system is optimized as a result. Any number of characters can be transferred.
PCI	Peripheral Component Interconnect – parallel bus from host to this device
PIM	PMC Interface Module (PIM). Provides rear I/O in cPCI systems. Mounts to PIM Carrier
PIM Carrier	PIM Mounting Device. Mounts on rear of cPCI backplane.
PMC	PCI Mezzanine Card – establishes common connectors, connections, size and other mechanical features.
TAP	Test Access Port – basically a multi-state port that can be controlled with JTAG [TMS, TDI, TDO, TCK]. The TAP States are the states in the State Machine that are controlled by the commands received over the JTAG link.
TCK	Test Clock provides synchronization for the TDI, TDO, and TMS signals

TDI	Test Data in – this serial line provides the data input to the device controlled by the TMS commands. For example, the data to program the FLASH comes on the TDI line while the commands to the state machine to move through the necessary states comes over TMS. Rising edge of TCK valid.
TDO	Test Data Out is the shifted data out. Valid on the falling edge of the TCK. Not all states output data.
TMS	Test Mode State – this serial line provides the state switching controls. '1' indicates to move to the next state, '0' means stay put in cases where delays can happen; otherwise, 0,2 are used to choose which branch to take. Due to the complexity of state manipulation, the instructions are usually precompiled. Rising edge of TCK valid.
UART	Universal Asynchronous Receiver Transmitter. Common serialized data transfer with start bit, stop bit, optional parity, optional 7/8 bit data. Can be over any electrical interface. RS232 and RS422 are most common.
Unpacked	When UART characters are sent on an unknown basis requiring single character storage and transfer over the host bus
VendorID	Manufacturers number for PCI/PCIe boards. DCBA is Dynamic Engineering's VendorID
VME	Versa Module European
VPX	Family of standards based on the VITA 46.0
XMC	Switched mezzanine card (PMC with PCIe)