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User Manual

PCIBPC104pET

PCI Bridged PC104p Compatible Carrier
Extended Temperature
Up to 4 Modules

Revision A
Corresponding Hardware: Revision A/B
Fab number10-2009-0701/2

PCIBPC104pET
PCI and PC104p Compatible Carrier

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Product Description

PCIBPC104pET is part of the Dynamic Engineering PCI and PC104p compatible family of modular I/O components.

PCIBPC104pET is a short PCI design with the ability to host up to 4 PC104p modules. PCI-104 cards are also compatible. The design is rated for industrial temperature operation “ET” –40C ⇔ +85C.

The bridge isolates the PCI bus from the local PC104p PCI bus allowing mixed frequency and width operation. VIO is programmable allowing mixed voltage definitions as well.

Easy to use as a plug and play device. In transparent mode no special software is required for the carrier. A special hidden address range is available to allow high-speed local bus operations without interfering with the PCI bus.

Special features:

- Universal PCI short [less than 1/2 length] board.
- Extended temperature range [-40 +85C]

LED names within quotes:

- LED on plus 12V “P12V”
- LED on minus 12V “M12V”
- LED on plus 5V “P5V”
- LED on plus 3.3V “P3.3V”
- LED on 1.8V “P1.8V”
- User selectable secondary VIO.
- 32 or 64 bit operation on PCI bus
- 66 or 33 MHz operation. With 66 MHz. primary bus speed the secondary bus can be 66 or 33 MHz. Secondary bus can be at a higher rate than the primary bus using oscillator option.
- Option for upper or lower address range used on IDSEL – switch setting.

The PCIBPC104pET is ready to use with the default settings. Just install the PC104p modules onto the PCIBPC104pET and then into the system. There are a few settings to optimize performance.

DipSwitch Settings

Revision 1 SW1 is marked with 1, 0 and SW2 is marked with C, 0.
Revision 2 both switches will be marked with C, O. C = closed, O = open

The quick reference tables on the board have the basics. Read below for additional information. For detailed information refer to the Bridge manual.

Please note: on revision 1 boards the SilkScreen has the positions for 1,0 reversed at SW1. The table for SW1 should be interpreted with the correct 1,0 positions. 0 is closed which happens to be in the "up" position and 1 is open which is the down position.

The following definitions reflect the Revision 2 silk with Closed and Open for SW1. Please substitute Up for closed and Down for Open for revision 1 boards.

DIPSWITCH #1 [SW1 table on silk-screen]
Select the "green power" clock setting. With the new revision of the bridge [PLX 6466] the secondary clock can be set to be driven low or continue to operate when in the power down state. With the **DIP switch 1** set to 'O' the clock will be driven low during power down, and with the switch 'C' the clock will always be driven. The factory setting is 'C'. **BPCC_EN** is the signal controlled with switch 1.

Select the Bridge "S_CLKOFF". The bridge can drive or not drive the CLK outputs. With a standard PC104p installed the clocks should be enabled. With **switch #2** set to 'C' the clocks are enabled, with the switch in position 'O' the clocks are disabled. **CLK_OFF** is the signal controlled with switch number 2. The factory setting is 'C'.

Select the Bridge "DEV64#". The bridge can accommodate 32 and 64 bit cards installed into the PC104p slot. With **switch #3** set to 'O' the bridge will read the installed PC104p(s) to be 32 bit. With the switch set to 'C' the bridge will report a 64 bit device. The factory setting is 'O'. Please note that the hardware will detect the ACK64# signal to determine the port width for transactions. Since current PC104p cards are all 32 bit this switch should always be in the Open position.

PBOOT is selected with **Switch #4**. When 'C' the secondary port is selected for "Boot Priority". When 'O' the primary port is selected. The PBOOT setting has meaning when in the non-transparent modes. The factory setting is 'O'.

MSK_IN is selected with **Switch #5**. When 'C' the Bridge clock outputs are enabled. When 'O'' the bridge clock outputs are disabled. Both Mask and Clock Off need to be enabled for normal operation. The factory setting is 'C'.

UMODE is selected with **Switch #6**. When '1' and in non-transparent mode the bridge will be configured to be a "universal bridge". The factory setting is 'C'.

TRANS# is selected with **Switch #7**. When 'C' the bridge will act in transparent mode. When 'O' the bridge will be in non-transparent mode. The factory setting is 'C'.

Select the secondary side [PC104p] PCI bus frequency. The options are to use the PCI bus speed [primary] or to force 33 MHz on the secondary side. The PC104p(s) to be installed must be 66 MHz compliant to use the 66 MHz secondary side option. The speed is controlled with the **DIP switch #8** position. 'O' = 66 MHz capable secondary side. 'C' = 33 MHz. **SM66EN** is the signal name controlled by the switch. The factory setting is 'C'. Please note: the PC104p modules also control this signal. Leaving in the "O" position will allow the modules to control the clock rate. Setting to "C" will force to 33 MHz.

Please note that the secondary side can operate at frequencies other than the PCI frequency by using the oscillator. For example the PCI speed can be 33 and the secondary side be 66 if the oscillator is used. The Bridge takes care of the rate matching and has large FIFO's. Please refer to the DIPSwitch #2 definitions.

DIPSWITCH #2 [SW2 table on silk-screen]

Switch #1 selects the secondary side VIO [**SVIO**]. When the switch = 'O' 3.3V is selected for the secondary side. When 'C' is selected 5V is the VIO definition. The VIO plane is a reference for the IO level. The specification does not prohibit larger current consumption from these pins. The PCIBPC104pET design utilizes a MOSFET to control the 5V or 3.3V rails onto the VIO plane. Max consumption on the VIO rail is 3A. The factory setting is 'O'.

Switch #2 selects the clock reference to use for the secondary side. "O' selects the PCI clock from the primary side and 'C' selects the installed oscillator. The oscillator has a default frequency of 66 MHz. Please note that the secondary side frequency still depends on the M66EN definition – the bridge will divide the clock if set to 33 capable. The factory setting is 'O'.

Switch #3 selects the addressing mode. When 'O' the Private memory space is selected for the secondary side, when 'C' the standard memory map is selected. The factory setting is 'C'. **PRVDEV/XBMEM** is the signal controlled by this switch. It is recommended to read the PLX manual on the 64/66 when this signal is to be used.

Switch #4 selects **Primary PLL** enabled or not. 'O' disables the PLL and 'C' enables the PLL. The factory setting is 'O'. If operating at 50 MHz or more on the primary side the PLL should be enabled. When operating below 50 MHz the PLL should not be enabled. At 33 MHz disable. At 66 MHz enable. For revision 2 and later boards this function will be automatic and SW2-4 will be "spare"

Switch #5 selects **Secondary PLL** enabled or not. 'O' disables the PLL and 'C' enables the PLL. The factory setting is 'O'. If operating at 50 MHz or more on the secondary side the PLL should be enabled. When operating below 50 MHz the PLL should not be enabled. At 33 MHz disable. At 66 MHz enable. For revision 2 and later boards this function will be automatic and SW2-4 will be "spare"

Switch #6 selects **PC104p IDSEL** range. 'C' selects the lower range with AD16-AD19. 'O' selects the upper range with AD20-AD23 The factory setting is 'C'.

Switch #7 Spare

Switch #8 Spare

Interrupts

Interrupts from the PC104p's are connected from the PC104p to the primary PCI bus. INTA through INTD are mapped directly to the primary bus segment . Each module will select its stack position. Based on stack position selection the IDSEL, CLOCK, REQ, GNT, and INT lines are defined.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
The PC104p modules are mounted to the PCIBPC104pET prior to installation within the chassis. For best results: make sure the PCI bracket is screwed down.

There are four mounting locations per PC104p. The PCIBPC104pET card supports all 4 locations. Standoff's are used between modules.

The PC104p Module connectors are keyed via the mounting holes. It is good practice to align the mounting holes before installing the Module. The PCI connector is symmetrical and it is possible to mount in reverse. When mounted properly all 4 hole locations will be in alignment.

The Stack can be grown in either direction – front to back or in front. The clocks are matched length on the PCIBPC104pET card by adding length to the presumed lower stack positions. Clock 3 is matched to the length of the other PCI signals propagated through the stack. Clock 2 is matched to Clock 3 and the stack offset added. Similarly Clock 1 and Clock 0 have additional offsets added.

The board closest to the PCIBPC104pET card is considered position 0 and the furthest position 3. Setting the installed modules with the same definitions can improve performance. There is enough margin in the PCI design to allow for non-optimal configurations.

Please note that you can use both sides of the PCIBPC104pET card . For balance and reduced overhang it may be better to mount some modules to the rear and some to the front. It is suggested the inner two modules are 0,1 and the outer 2 or stacked 3 become the remaining addresses, For example: 0⇔PCIBPC104pET⇔1,2,3 or 2,0⇔PCIBPC104pET⇔1,3.

Start-up
A third party PCI device cataloging tool will be helpful to check that the VendorID and CardID are "seen" by the OS.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCIBPC104pET when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the PC104p modules installed into the PCIBPC104pET more than the PCIBPC104pET itself, and it is smart system design when it can be achieved.

Construction and Reliability

The PCIBPC104pET is constructed out of 0.062 high temp ROHS compliant material. Gold has been used for plating rather than Tin for improved performance over time. “leaded or unleaded” components can be used along with solder choices. Dynamic Engineering can support both processes.

Surface mounted components are used. The connectors are through hole [compression fit] for the PC104p. Gold plated pins on both plugs and receptacles. They are rated at 1+ Amp per pin..

The PC104p Modules are secured against the carrier with the PC104p connectors. It is recommended, for enhanced security against vibration, that the PC104p’s mounting screws and standoff’s are installed. The screws/standoffs are supplied with the PC104p from the OEM. Dynamic Engineering has screws, standoffs, and other PC104p hardware available at a reasonable cost if your PC104p was not shipped with some of the required attachment hardware or if it has been misplaced.

Thermal Considerations

If the PC104p modules installed have a large heat dissipation; forced air cooling is recommended.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $125. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

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Specifications

Logic Interfaces:	PCI Interface 33/32 ⇔ 66/64
Access types:	PCI bus accesses
CLK rates supported:	33 or 66 MHz PCI clock rates
Software Interface:	transparent Bridge. PLX6466 registers in configuration space
Initialization:	Selections for VIO, primary and secondary clock rates
Interface:	PC104p connectors supplied with modules.
Dimensions:	PCI short – less than 1/2 length PCI card.
Construction:	High Temp ROHS compliant Multi-Layer Printed Circuit board, Through Hole and Surface Mount Components. Add –ROHS for ROHS processing.

Order Information

standard temperature range –40 ⇔ +85ºC

PCIBPC104pET	PCI card with PC104p stack position http://www.dyneng.com/pcibpc104pet.html
-CC	Conformal Coating is available as an option.
-ROHS	Add for ROHS processing.