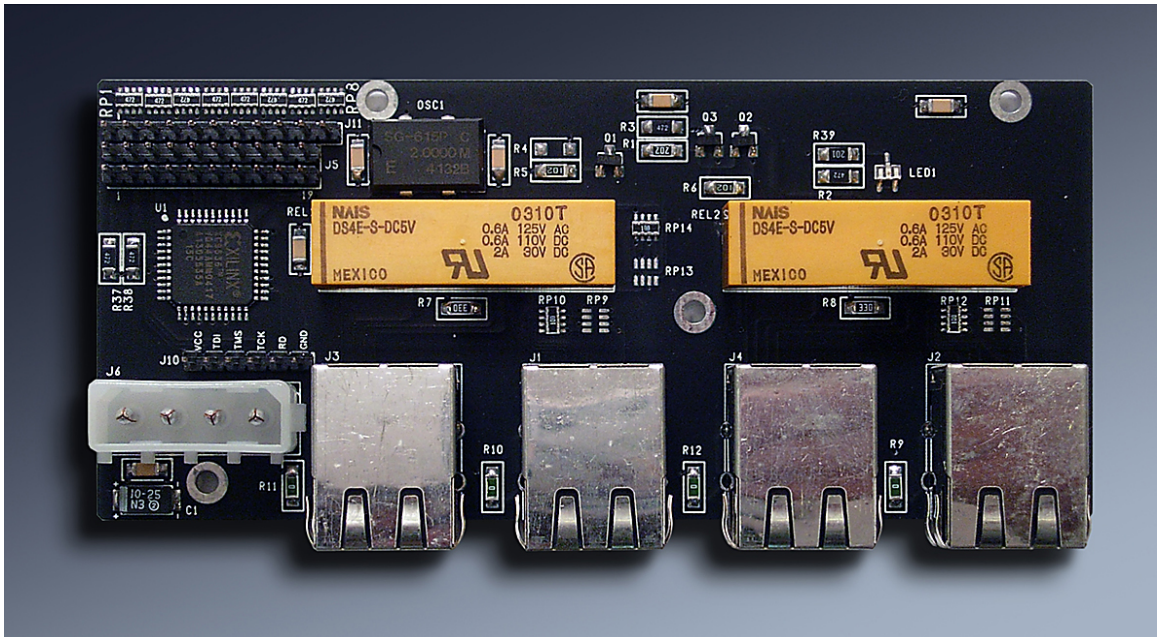
DYNAMIC ENGINEERING
150 DuBois St. Suite B&C, Santa Cruz CA 95060
831-457-8891
sales@dyneng.com www.dyneng.com
Est. 1988

User Manual

Stand-Alone-Relay
S-A-Relay



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S-A-Relay

Dynamic Engineering
150 DuBois St.
Suite B&C
Santa Cruz, CA 95060
831- 457-8891

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PC's and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

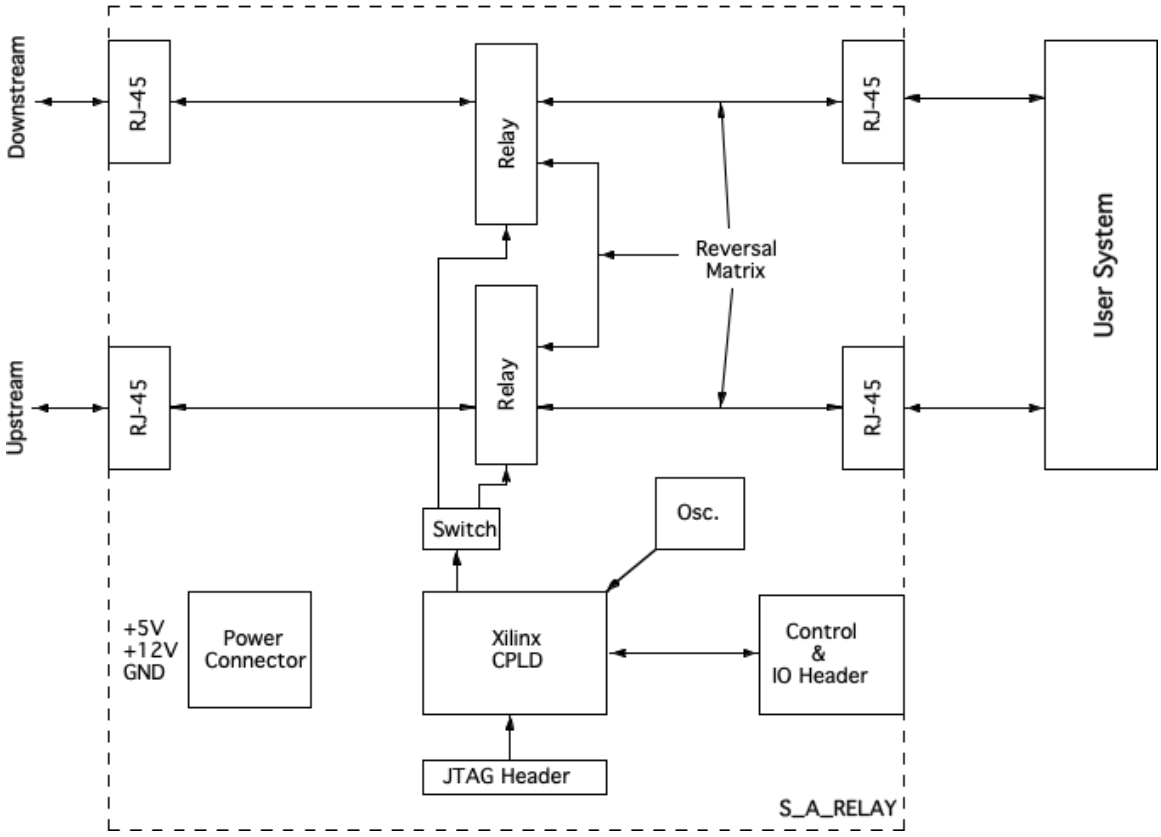

FIGURE 1 S-A-RELAY BLOCK DIAGRAM

The S-A-Relay was designed to provide the capability of intercepting Ethernet signaling. The signal interception could be for data compression, analysis, regulation, etc. ISPs demand signal integrity and fail-safe operation. The S-A-Relay “fails” in the bi-pass mode where the upstream and downstream lines are interconnected. If Power fails, the user system disables the SW_CNTL or Reset is asserted the S-A-Relay will automatically return to the bi-pass mode taking the user system out of the “system”.

The S-A-Relay has options to account for system wiring differences. The reversal matrix can be used to account for RX-TX wiring differences. The default works in most systems. The default is reversed between the relays and pass

between the user system and relays. Please advise Dynamic Engineering if you need alternate interconnections implemented in assembly.

The CPLD is a Xilinx 9536. The 9536 is programmable via the JTAG header and comes preprogrammed with the standard algorithm. There are two headers with 21 uncommitted IO. The user or Dynamic Engineering can implement alternate programs within the 9536 to control the relays. The engineering kit comes with the base design implemented in VHDL.

Base Logic:

When Resetn is asserted low goto IDLE from any state.

When IDLE remain in IDLE until SW_CNTL =‘0’ - Bi-pass mode
goto S0 when SW_CNTL = ‘0’

When S0 remain in S0 until SW_CNTL is detected ‘1’ – Bi-pass mode
Goto S1 when SW_CNTL = ‘1’

When S1 remain in S1 if SW_CNTL = ‘1’ and count ≠ 3d0900 – Bi-pass
Goto S2 if SW_CNTL = ‘0’
GoTo Relay On if SW_CNTL = ‘1’ and count = 3d0900

When S2 remain in S2 until SW_CNTL = ‘1’ - Bi-pass mode
Goto S1 when SW_CNTL = ‘1’

When Relay On remain in Relay On until SW_CNTL = ‘0’ Active mode
Goto S2 when SW_CNTL = ‘0’

The hardware resets to idle with the relays not energized causing the Ethernet signals to be routed from input to output directly. Once Resetn is released the hardware will wait for SW_CNTL to be low [inactive] before going to the next state. The pull-down on the board and the active detection of a transition from off to on protects against in-advertent Active mode operation. Once the SW_CNTL signal is activated the hardware progresses to state S1 where it waits for the counter to progress to 0x3d0900. [2 MHz reference with 3d0900 creates a 2 second delay]. The delay with the control in the high state insures against a noisy system causing apparent transitions on the SW_CNTL line. Once the delay is satisfied the hardware progresses to the active state [Relay On]. If the terminal count is not satisfied before the SW_CNTL line is detected low then the hardware clears the count and waits for SW_CNTL to go active again.

Once in the Relay On state the relays are activated via a power control circuit. The Relays will remain activated until the SW_CNTL is set to inactive or RESETN is asserted.

LED1 will be energized when the RELAYs have power applied.

J1-4 are rated for 10/100 operation as well as the relays and board routing. The connector J3 is considered the Upstream and J4 the Downstream connector. When in Bi-pass mode J3 is connected to J4 via the reversal matrix. When in Active mode J3 is connected to J1 and J4 is connected to J2. The user equipment should take the signals from J1 and repeat or replace them on J2 as needed by your architecture.

J10

Pin	Name
1	VCC
2	TDI
3	TMS
4	TCK
5	TDO – marked RD on Xilinx Parallel Port Programmer
6	GND

FIGURE 2 S-A-RELAY JTAG [J10] PINOUT

The JTAG connector is used to program the CPLD. With the use of the Xilinx Foundation package and the “Impact” programming software the design file can be programmed into the CPLD in circuit. Connect the programmer flying leads as indicated in the silk-screen.

J6

Pin	Name
1	VCC
2	GND
3	GND
4	+12V [not connected on board]

FIGURE 3 S-A-RELAY POWER [J6] PINOUT

The Power Connector matches a standard HDD power cable to allow ease of connection within a PC.

J5

Pin	Name
1	SW_CNTL
2	spare
3	RESETN
4-20	spare

FIGURE 4 S-A-RELAY CONTROL [J5] PINOUT

When SW_CNTL = '1' and RESETN = '1' the relay will initialize and go to the active mode. When SW_CNTL = '0' or RESETN = '0' the relay will go to Bi-pass mode. For more details see the Product description discussion.

J5 is a 2x10 header with .025" sq. posts. Pins 1 and 19 are marked. All spare pins are terminated with 4.7K pull-ups. SW_CNTL and RESETN are terminated with 4.7KΩ pull-downs. All pins are connected to the CPLD.

J11

Pin	Name
1-11	SPARE

FIGURE 5 S-A-RELAY SPARE [J11] PINOUT

J11 is a 1x11 header with .025" sq. posts. Pins 1 is aligned with J5 pin 1. All pins are terminated with 4.7K pull-ups. All pins are connected to the CPLD.

J5 and J11 are for user expansion.

J1,2,3,4

Pin	Name
1	TDS+
2	TDS-
3	RDS+
6	RDS-
4,5,8	open

FIGURE 6 S-A-RELAY RJ-45 [J1-4] PINOUT

J1-4 are standard 10/100 RJ-45 jacks suitable for Ethernet connections.

Construction and Reliability

The S-A-Relay was conceived and engineered for rugged industrial environments. The S-A-Relay is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used.

The S-A-Relay can be secured against a mounting plate with standoffs. There are four mounting holes provided for this purpose.

The S-A-Relay Module provides a low temperature coefficient for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C. The S-A-Relay is a low power device with a lot of surface area relative to the thermal load. In most environments no additional airflow will be required.

Thermal Considerations

The S-A-Relay design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one-degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

https://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite B&C
Santa Cruz, CA 95060
831-457-8891
support@dyneng.com

Order Information

S-A-Relay	S-A-Relay module with built in 10/100 ethernet switch network and control logic. User control via SW_CNTL input. System control via RESETN input.
Eng Kit–S-A-Relay	Design Directory – VHDL files plus UCF and project. Schematic of S-A-Relay. Data sheet reprints are available from the manufacturer's web site reference software.

***Note**: The Engineering Kit is strongly recommended for engineers planning to modify the programming within the S-A-Relay.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.