DYNAMIC ENGINEERING
435 Park Dr., Ben Lomond, Calif. 95005
831-336-8891 **Fax** 831-336-3840
sales@dyneng.com
www.dyneng.com
Est. 1988

User Manual

IP-CARA

CARA Network Interface Independent Transmit and Receive Channels

IndustryPack® Module

Manual Revision A1
Corresponding Hardware: Revision B
PROM revision A
FAB NO. 10-2004-0402

IP-CARA
Controller Area Network Interface
IndustryPack® Module

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised 12/13/2006.

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Product Description

IP-CARA is part of the IndustryPack® “IP” Module family of modular I/O components by Dynamic Engineering. IP-CARA provides independent transmit and receive channels. The IO is based upon the ARINC-429 standard. The data format is “CARA”. 24 bits send LSB first. Tristate transmitter when not active. Tri-level logic to define the data.

The transmit side is has a programmable reference clock rate based on a 32 MHz oscillator. The desired rate x2 is programmed into the clock generator. Each period of the reference clock is used to output the control pattern to the 429 transmitter. Tristate, NULL, data ‘1’ or data ‘0’ are the possibilities. Each bit period consists of a bit and a Null.

The data is stored into a FIFO built out of Block RAM within the Xilinx. The FIFO stores the data as 16 bit words. The lower 16 bits are written first and the upper byte second for the 24 bits transmitted. Multiple words can be stored and sent one at a time or as a group with a programmable delay between words.

The transmitter stays in the Hi-z mode until the start bit is set. The Hardware then drives the data bus with a Null followed by the first bit. Nulls followed by data continue for the 24 bits. A final Null is driven and then the bus returned to Hi-Z.

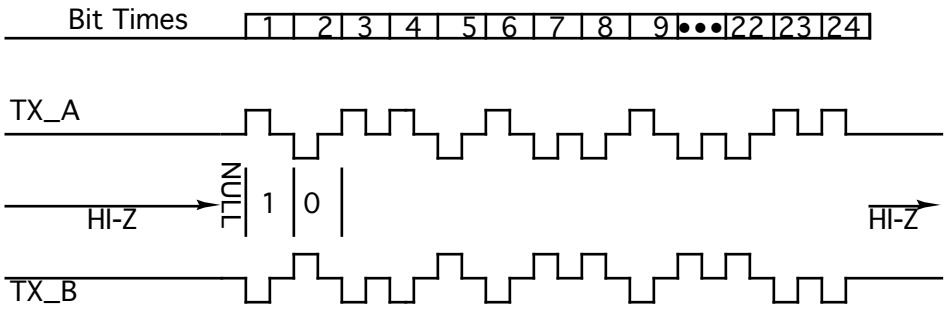


FIGURE 1 IP-CARA TIMING DIAGRAM

Software can load more than 1 word to transmit into the FIFO. The data can then be sent with new start commands, or under hardware control. With hardware control the software can program a delay time between words based on the transmit clock. Interrupts can be generated for each word or when the last word is sent [TX FIFO MT]

The receive side when enabled will look for a non-data gap before starting to capture data. The gap requirement is programmable. If set to 2 periods or more active data will not be present meaning that a word is not being transmitted. Once the gap is detected the hardware waits for valid data to be received and captures 24 bits before rearming for the next word. Captured data is stored into a FIFO. Interrupts can be generated for each word received.

The IP interface is 8 and 32 MHz compatible.

IP-CARA is an adaptation of the IP-QuadUART design. The UART and transceivers are left off and the ARINC 429 transmitter and receiver added back as rework. Plans are in the works for a new IP-429 design using the same transmitter and receiver parts as IP-CARA. IP-CARA can be updated to make use of the new IP-429 design.

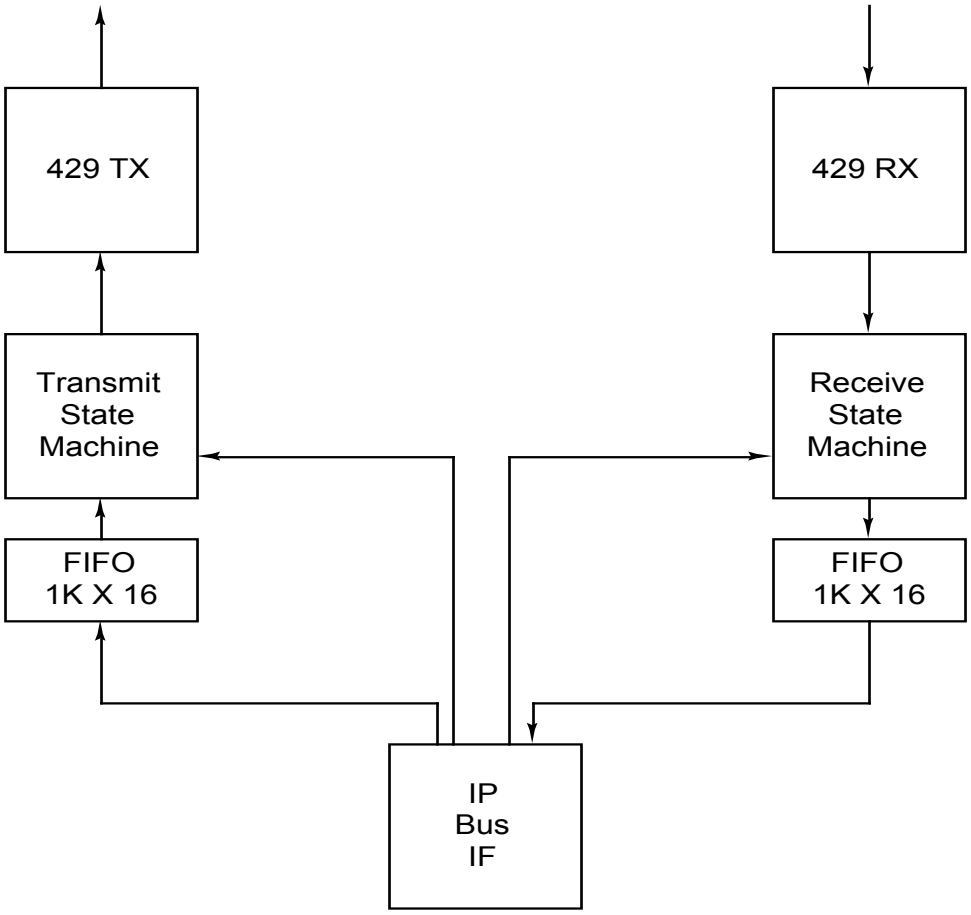


FIGURE 2 IP-CARA BLOCK DIAGRAM

All FPGA configuration registers support read and write operations for maximum software convenience.

IP-CARA conforms to the IndustryPack® standard. This guarantees compatibility with compliant carrier boards. Because IP-CARA may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCI3IP – PCI carrier for IP Modules can be used for development in a conventional PC. Later the hardware and software can be ported to the target.
http://www.dyneng.com/pci_3_ip.html

With the Dynamic Engineering Windows driver collection for IP and carrier modules a Parent – Child architecture is employed. The IP portion of the driver is directly portable between the various Dynamic Engineering IP carriers [PCI3IP, PCI5IP, PC104pIP, PC104p4IP, cPCI2IP, cPCi4IP etc]. The parent portion of the driver contains the carrier specific design information. This means that software developed for the IP-CARA on one platform can be directly ported to another. PCI to cPCI for example.

Designers can even make use of the Dynamic Engineering carrier driver for non Dynamic Engineering IP modules using the Generic IP capability built into the parent portion of the driver. IP modules that the carrier driver does not recognize are installed as “generic” and accessed with a address, data interface model. Software developed for the Generic mode can also be ported between modules.

IP-CARA is tested with a combination of internal and external tests. The registers can be tested with R/W tests, and the channels can be tested with loop-back. The ATP for IP-CARA includes internal, and loop-back tests.

Interrupts are supported by IP-CARA. Each channel has a separate interrupt and enable. In addition a board level SW interrupt is provided for test and software development purposes.

IP-CARA is implemented with the idea of offloading the CPU as much as possible. The internal FIFOs to cut down on the number of interrupts to deal with. Most registers retain their information between messages allowing for quick reload and send once the initial programming has been implemented.

Address Maps

Address Map Internal

```
IP_CARA_BASE        0x0000  // 0 base control register offset
IP_CARA_VECTOR      0x0002  // 1 Vector Register offset
IP_CARA_STATUS      0x0004  // 2 Base Status register
IP_CARA_ControlTx   0x0014  // 10 TX control register
IP_CARA_TXSP        0x0016  // 11 TX Speed register
IP_CARA_FIFO_TX     0x0018  // 12 TX FIFO
IP_CARA_ControlRx   0x0028  // 20 RX control register
IP_CARA_FIFO_RX     0x002C // 22 RX FIFO
```

FIGURE 3 IP-CARA INTERNAL ADDRESS MAP

Programming

Programming IP-CARA requires only the ability to read and write data from the host. The base address refers to the first user address for the slot in which the IP is installed.

Depending on the software environment it may be necessary to set-up the system software with IP-CARA "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware. Other OS may be more “plug and play”. The Dynamic Engineering Driver operates in a “plug and play” mode with a parent ⇔ child architecture.

In order to receive and or transmit data the software is required to enable the controller for the channel(s) of interest. The initialization procedure is a mult-step process. To transmit the TXSP register is set to the frequency of interest, data is loaded into the FIFO and then the start bit set. To receive the start bit is set and the data read from the FIFO when data has been captured.

Interrupts are used to help manage the data transfer process. When a programmed transfer is completed the interrupt can be generated to alert the host to program a new transfer. The transfers are independent for each channel allowing the CPU interaction to be minimized.

Register Definitions

IP_CARA_BASE

IP_CARA_BASE 0x0000 // 0 base control register offset

BASE Control Register

DATA BIT	DESCRIPTION
15-9	Spare
8	Reset RX
7-5	Spare
4	Reset TX
3-1	Spare
0	INTFORCE

FIGURE 4 IP-CARA BASE CONTROL REGISTER BIT MAP

Intforce when set causes an interrupt to be generated to the system. Useful for debugging and software test.

Reset RX and Reset TX when set [‘1’] cause a reset of the respective FIFO and state-machine. The Reset bits are combined with the system reset to make a local reset which is also active for global reset conditions – Power on and IP reset.

The RX state-machine has conditions in each of the “waiting” states to check the state of the start bit. Reset Rx will cause a forced reset to the idle state and dump the FIFO contents. Clearing the Start bit will cause the RX state-machine to return to IDLE and not reset the FIFO. The control registers are not affected by the reset bit.

The TX State-machine and TX FIFO are reset by Reset TX. The reset acts as a hardware reset forcing the state-machine back to idle and dumping the contents of the FIFO. The control registers are not affected by this reset.

IP_CARA_VECTOR

IP_CARA_Vector 0x0002 // 1 IP vector port

Vector Port

DATA BIT	DESCRIPTION
15-8	Spare
7-0	switch in

FIGURE 5 IP-CARA VECTOR BIT MAP

If the system uses a vectored interrupt approach then the vector port should be initialized to the vector value assigned to this device. IP-CARA is designed to be used as vectored or auto-vectored. In auto-vectored situations this port is unused. The Status port can be used to determine the source of any pending interrupts from IP-CARA.

IP_CARA_STATUS

IP_CARA_STATUS 0x0004 // 2 base Status register

CONTROL RX

DATA BIT	DESCRIPTION
15-8	Spare
7	RX FULL
6	RX MT
5	TX FULL
4	TX MT
3	RX OVERFLOW
2	RX INT
1	TX INT
0	LOC_INT

FIGURE 6 IP-CARA INTERRUPT STATUS BIT MAP

LOC_INT is set when INTFORCE, TX_INT or RX_INT are set and the corresponding mask is enabled. This bit is cleared by dealing with the interrupt source.

The TX and RX INT signals are set high when the programmed events occur. In the case of TX the interrupt can be set per word sent or when the last word is sent. In the case of RX the interrupt happens each time a word is received. In most cases with the CARA protocol there is a significant delay between words sent or received.

RX Overflow is set when the RX FIFO is full and it is time to write another word to the memory.

The RX INT, TX INT, and RX Overflow bits are held until explicitly cleared by writing to this register with those bits set.

The FIFO status is available. Active high. TX and RX MT will be set after a reset or when ever the FIFOs are empty. The Full bits will be set when the FIFOs are filled to capacity.

IP_CARA_ControlTx

IP_CARA_ControlTx 0x0014 // 10

Tx Control REGISTER

DATA BIT	DESCRIPTION
15	Interrupt Mask
14	TX MT INT
13	TX Clear Start Enable
12	TX Enable
11-0	TX CNT

FIGURE 7 IP-CARA TX CONTROL BIT MAP

Interrupt Mask when set '1' enables the channel interrupt to cause an IP level interrupt. When '0' the interrupt from the channel can still be used as a status bit, and the interrupt will not cause an IP level interrupt.

TX CNT is used to determine how much time to delay between sending words of data. This count is applied at the end of a transmission. The count has an effective value based on the TX clock reference rate selected with the TXSP register.

With the count set to 0 a delay of 7 periods will happen before coming out of Hi-Z. With the count set to 1 the delay is 10. Additional delays happen linearly with the count. For a count n>1 the delay will be (n-1)*T + 10*T.

429 interfaces frequently use 12.8 KHz as a transmission rate. The TX reference rate is 2X the transmission rate or 25.6 KHz in this example. T = 39.1 uS. With N= 2 the offset will be 429.7 uS. With 12 bits up to 4095 can be programmed for an effective delay of 4104 or ~160 mS at with the example clock rate.

TX Enable when set causes the transmitter to start sending data. The state-machine will read the first two words from the FIFO and load the shift register. The state-machine will control the bus to not be in hi-z, drive a null, and then start putting out data bits interspersed with nulls. At the end of the word the state-machine will assert the "clear start" signal.

Clear Start is conditioned with TX CLEAR Start Enable and TX MT INT to determine if the start bit should be automatically cleared at the end of the current word sent or not.

When TX CLEAR Start Enable is set [‘1’] the Start bit will be cleared at the end of a word sent. The word that causes the clear is determined by the TX MT INT bit. If set then the word sent when the TX FIFO is MT will cause the clear to the Start Bit. Setting both bits would be used when doing a multiple word transfer using hardware timing control. When one word is to be sent at a time the TX MT INT bit would not be set to cause the clear on each word.

The “pre-mask” interrupt will happen at the end or on each word. When TX MT INT is set the interrupt happens at the end based on the TX FIFO MT signal. When cleared the interrupt happens on each word.

The pre-mask interrupt is captured and held in the status register. If the Interrupt Mask is set the status will also drive an interrupt request. The status bit can be used to poll if the mask is not enabled.

IP_CARA_TXSP

IP_CARA_TXSP 0x0016 // 11

Tx Control REGISTER

DATA BIT	DESCRIPTION
15	HiLo
14-12	Spare
11-0	TX Speed

FIGURE 8 IP-CARA TX SPEED BIT MAP

TX Speed sets the transmission speed for the TX channel. The formula is 2(n+1) for the divisor based on a 32 MHz clock. The TX bit rate is half of this reference. For 12.8KHz program 25.6 KHz. 32MHz/25.6KHz = 1250 => n= 624 or 0x270.

The HiLo bit is set or cleared to control the shape of the waveforms on the IO. 0 = low speed and 1 = “high” speed. Low speed for frequencies at the lower end of the 429 range ~10-15 KHz. High speed at the upper end of the range 100 KHz etc.

IP_CARA_FIFO_TX

IP_CARA_FIFO_TX 0x0018 // 12

TX FIFO	
DATA BIT	**DESCRIPTION**
15-0	TX Data – Write only

FIGURE 9 IP-CARA TX FIFO BIT MAP

The data to transmit is written to this port. The data is written to a FIFO. The address is constant. The data is x16. Data is loaded lower 16 then upper 8. The upper 8 are LSB aligned [as if writing a 32 bit word lower half then upper half].

IP_CARA_ControlRx

IP_CARA_ControlRx 0x0028 // 20

Tx Control REGISTER	
DATA BIT	**DESCRIPTION**
15	Interrupt Mask
14	Spare
13	RX Clear Start Enable
12	RX Enable
11-0	RX CNT

FIGURE 10 IP-CARA TX CONTROL BIT MAP

RX CNT is used to determine how much time to wait receiving NULL or HI-Z before determining that no transmission is currently taking place. The idea is to wait long enough to insure that the data captured is a complete word and not part of a word. This count is checked at the start of each word. The count has an effective value based on the 32 MHz clock reference rate. It is suggested that a count equivalent to a couple of bit periods is used for the synchronization. 32MHz/12.8KHz = 2500 per bit period at the 21.8 KHz rate. 0x1388 would be two bit periods. Longer or shorter values can be used based on your system requirements.

RX Enable when set causes the receiver to start looking for data. The state-machine will check for the sync time of non-data then start to capture bits. At the end of the word [24 bits] the state-machine will assert the “clear start” signal.

Clear Start is conditioned with RX CLEAR Start Enable to determine if the start bit should be automatically cleared at the end of the current word sent or not. If the start bit is auto cleared then the hardware will capture one and then disarm. If not enabled then all words will be captured until software disables the start bit.

The clear start signal will cause an interrupt request at the status register level for each word received. If the Interrupt Mask is set the status will also drive an interrupt request. The status bit can be used to poll if the mask is not enabled.

IP_CARA_FIFO_RX

IP_CARA_FIFO_RX 0x002C // 22

TX FIFO	
DATA BIT	**DESCRIPTION**
15-0	RX Data Read only

FIGURE 11 IP-CARA TX FIFO BIT MAP

The data received is written to this FIFO. The address is constant. The data is x16. Data is loaded lower 16 then upper 8. The upper 8 are LSB aligned [as if reading a 32 bit word lower half then upper half].

Interrupts

IP-CARA interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with an IP-CARA interrupt the software must read the status register(s) to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

The interrupt is mapped to INT0 on the IP connector, which is mapped to a system interrupt via the host [carrier] device. The source of the interrupt is obtained by reading the Interrupt Status register. The status remains valid until that bit in the status register is cleared.

When an interrupt occurs, the Master channel interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the status and enable the channel interrupt again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the Interrupt Status register.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable with the following pins connected. Channel 0 to Channel 1

SIGNALs	TX	RX
CARA_A	4	14
CARA_B	2	15

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IPs I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically.

Standard data in the ID PROM on the IP-CARA is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($06) IP-CARA
0D	Revision	($A0)
0F	reserved	($02) Customer Number
11	Driver ID, low byte	($01) Design Number
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($F8)

FIGURE 12 IP-CARA ID PROM

IP-CARA Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-CARA. Pins marked n/c below are defined by the specification, but not used on the IP-CARA. Also see the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		n/c		5		30	
	D2		MEMSEL*		6		31
D3		n/c		7		32	
	D4		INTSEL*		8		33
D5		n/c		9		34	
	D6		IOSEL*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		INTREG0*		17		42	
	D14		A4		18		43
D15		n/c		19		44	
	BS0*		A5		20		45
BS1*		n/c		21		46	
	n/c		A6		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		GND		25		50	

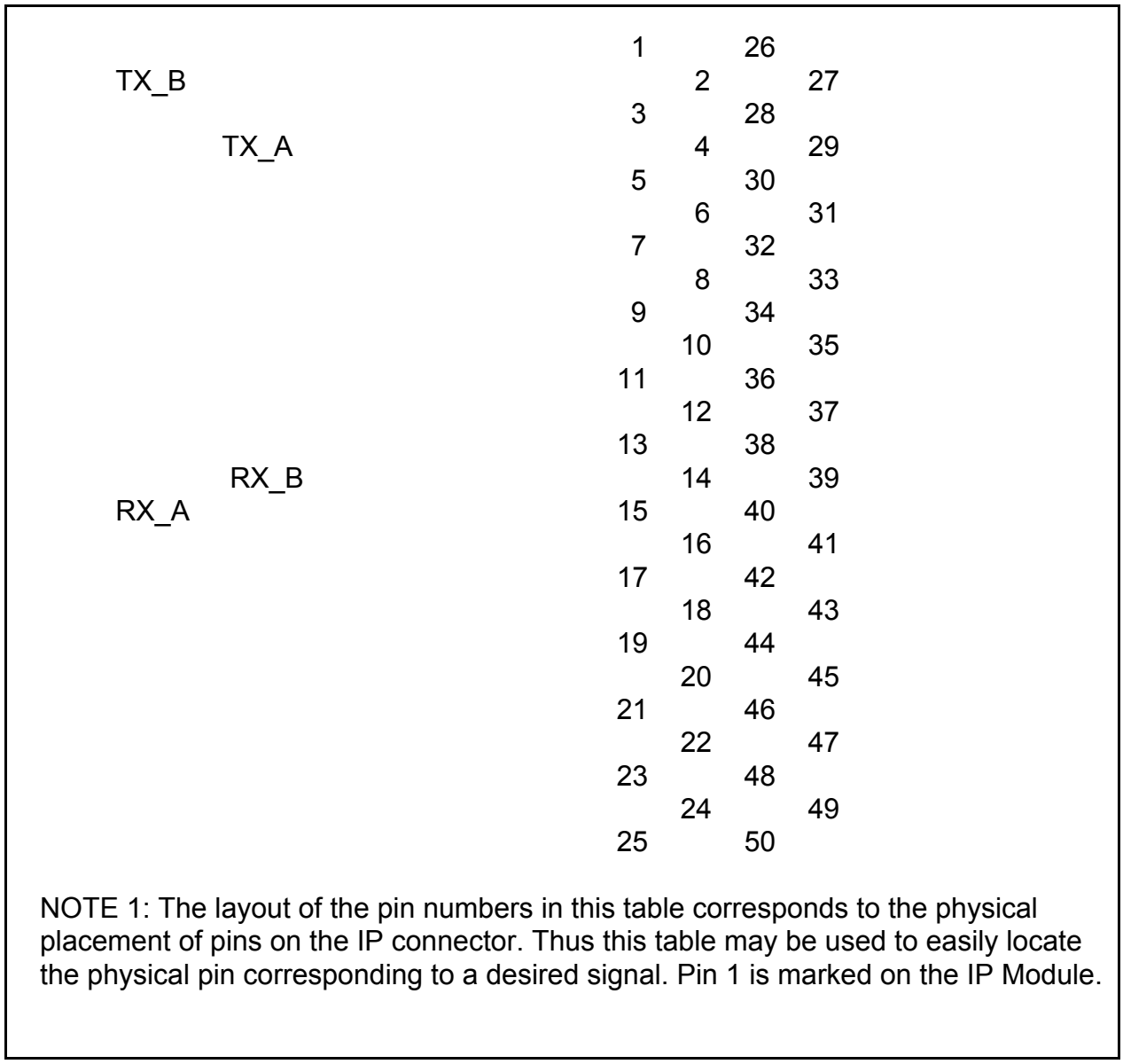
NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 13 IP-CARA LOGIC INTERFACE

IP-CARA IO Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-OPTOISO-16. Also see the User Manual for your carrier board for more information.



NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

FIGURE 14 IP-CARA IO CONNECTOR PINOUT

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs should be connected with standard CAN cabling or twisted pair wiring for best results.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the IP-CARA when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, use the isolated version.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-CARA does not contain special input protection. The connector is pinned out for a standard Header cable to be used. The twisted pairs are defined to match up with the IP-CARA pin definitions. It is suggested that this standard cable be used for most of the cable run.

Custom cables can be manufactured with discrete wire header and direct connection to your mating equipment.

Terminal Block. We offer a high quality 50-screw terminal block that directly connects to the ribbon cable. The terminal block can mount on standard DIN rails. HDRterm50 [http://www.dyneng.com/HDRterm50.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the CAN devices rated voltages.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-CARA is constructed out of 0.062 inch thick high temp FR4 material.

Through hole and surface mounting of components are used. IC sockets use screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of .89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if .89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-CARA design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
support@dyneng.com

Specifications

Host Interface:	IP Module 8 and 32 MHz capable
CARA Interface:	TX and RX independent channels
TX Data rates generated:	Programmable. 32 MHz reference with divider
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	IO, ID, INT spaces (see memory map)
Wait States:	1 added for FIFO access
Interrupt:	Channel interrupt for each CARA channel Software interrupt
Onboard Options:	Most Options are Software Programmable. Build options for isolated IO and reference grounds.
Interface Options:	IP IO connector routed through IP Carrier. Twisted pair cable recommended
Dimensions:	Type 1 IP Module.
Construction:	High temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	.89 W/^{o}C for uniform heat across IP
Power:	Typical **XX**mA @ 5V running channel to channel test

Order Information

IP-CARA	IP Module with TX and RX CARA channels
Tools for IP-CARA	IP-Debug-Bus - IP Bus interface extender http://www.dyneng.com/ipdbgbus.html IP--Debug-IO - IO connector breakout http://www.dyneng.com/ipdbgio.html
Eng Kit–IP-CARA	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender Technical Documentation, 1. IP-CARA Schematic 2. IP-CARA Reference test software Data sheet reprints are available from the manufacturer's web site reference software.

***Note**: The Engineering Kit is strongly recommended for first time* IP-CARA *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not guaranteed to be current or complete manufacturing data, nor is it part of the product specification.